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Encapsulamento de circuitos ópticos integrados
Packaging of Photonic Integrated Circuits

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor Mário Lima, Professor do Departamento de Eletrónica Telecomunicações e Informática da Universidade de Aveiro e do Engenheiro Francisco Rodrigues da PICAdvanced S.A.

Dedico este trabalho aos meus pais Joaquim e Fernanda e ao meu irmão Igor.

o júri

presidente	Professor Doutor José Rodrigues Ferreira da Rocha Professor Catedrático da Universidade de Aveiro
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agradecimentos

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palavras-chave Chip, encapsulamento, PIC, fibra, acoplamento ótico, *wire-bonding*, *flip-chip*

resumo

Com a constante evolução dos sistemas de comunicação óticos veio a necessidade de componentes optoelectrónicos de elevada performance a custos relativamente baixos. O encapsulamento ótico tem um papel chave nos dispositivos óticos de última geração.

Neste trabalho são descritas as regras de um processo de encapsulamento padrão, que abrange tanto o encapsulamento elétrico e ótico onde são exploradas técnicas de ajustamento ativas e passivas bem como o controlo térmico do circuito ótico integrado (PIC).

No início foi efetuado um processo de acoplamento da fibra ao chip com fibras de lente esférica personalizadas, numa primeira usando um chip de teste e de seguida num caso de estudo prático que consiste numa estrutura composta por um *holder* de silício com um laser de realimentação distribuída (DFB). É abordado em detalhe o processo de fabricação de *V-grooves* para o alinhamento da fibra com o chip.

De seguida são apresentadas e discutidas as técnicas de *wire-bonding* e *flip-chip* para o encapsulamento elétrico e ligação dos conectores de radiofrequência (RF), é feito um estudo onde são apresentados os resultados da caraterização dos parâmetros S de um PIC com *wire-bonding*.

Para o controlo térmico do módulo é apresentada uma técnica baseada em sensores de temperatura de ruténio e sensores de Platina e titânio testada numa PCB personalizada

keywords Chip, packaging, PIC, fiber, optical coupling, wire-bonding, flip-chip

abstract

With the continuous evolution of optical communication systems, emerged a need for high-performance optoelectronic elements at lower costs. Photonic packaging plays a key role for the next-generation of optical devices.

In this work a standard packaging design rules is described, covering both the electrical and optical-packaging exploring both active and passive adjusting techniques, as well as the thermal management of the photonic integrated circuit (PIC).

First a process for fiber-to-chip coupling with custom made ball-lensed fibers, is performed and tested initially in a testing-chip and thereafter in a manufactured practical study-case composed by a silicon holder with an InP distributed feedback (DFB) laser. The process of manufacturing etched V-grooves for fiber alignment is approached in detail.

After this, for electrical interconnects and radio frequency (RF) packaging, both wire-bonding and flip-chip technique are discussed, and a characterization of the s-parameters in a PIC with wire-bonding is presented.

A technique based on ruthenium-based sensors and platinum and titanium-based sensors for thermal control of the PIC is studied and the tested using a custom made PCB designed exclusively for that purpose.

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List of Acronyms

PIC	Photonic Integrated Circuit
PCB	Printed Circuit Board
PDR	Packaging Design Rules
LIGA	Lithography, Electroplating and Impression
Si	Silicon
InP	Indium Phosphide
AOI	Angle of Incidence
GC	Grating-coupler
PG	Pitch of the grating-coupler
SSC	Spot Size Converter
EIC	Electronic inter-connects
DC	Direct Current
RF	Radio Frequency
PDC	Pitch between DC bond-pads
PRF	Pitch between RF bond-pads
PPCB	Pitch of RF lines on a PCB
CPB	Solder-ball-bump
SBB	Copper-pillar-bump
SOA	Semiconductor optical amplifier
TEC	Thermo-Electric Cooler
CoP	Coefficient of Performance
SMF	Single Mode Fiber
WDM	Wavelength-division multiplexing
FPS	Fiber Processing Software
DFB	Distributed Feedback
PM	Phase modulator
MMI	Multimode interferometer
MOP	Maximum Optical Power
OP	Optical Power
UV	Ultra-Violet

KOH	Potassium Hydroxide
RIE	Reactive ion etching
DI	Deionization
Cr	Chromium
Si_3N_4	Silicon nitride
Al	Aluminum
Cu	Copper
Au	Gold chemical symbol
VNA	Virtual Network Analyzer
AWG	Array Waveguide Grating
PIN	P-I-N photodiode
PGM	Platinum group metals
Ru	Ruthenium
Pt	Platinum
Ti	Titanium
TCR	Temperature coefficient of electrical resistivity

1 Introduction

1.1 Context and Motivation

In the last 20 years (approx.) optical communication systems and the optical packaging technology have achieved a higher significance for general communications around the world [1]. Photonic integrated circuits (PICs) consist of combining optical components e.g. transmitters and receivers into a single chip allowing significant equipment cost savings as well as lower power consumption [2].

The last decade has seen the emergence of silicon photonics as a vehicle for the next-generation data communication technology [3].

On the other hand Photonic packaging covers the optical and electronic-coupling of photonic integrated circuits to the environment and it is becoming of great importance for the next generation of optical components to ensure low-cost, high performance and high-volume manufacturing [4] and shows itself as the most significant bottleneck in the development of commercially relevant integrated photonic devices [5].

To ensure that PICs can be packaged efficiently it is important to follow some basic packaging design rules to an easier and correct packaging and drives down the cost. These packaging rules specify the recommended dimensions, locations and orientations of the optical and electronic ports of the PIC. The packaging design flow follows three different areas such as, the optical design, the electrical design and thermal management of the module.

Fiber-to-chip coupling and electronic interconnect processes present the major technological challenges that have a major influence in the overall cost of the photonic module [1] as one of the main barriers to the commercial success of integrated photonic devices is the need for efficient, low-cost and packagable optical connections between a PIC and external fibers [3], also thermal management can compromise the performance of the device leading to an impact on reliability.

1.2 Objectives

The main scope of this thesis is to study the process of packaging of photonic integrated circuits. To do so, this thesis explores the following objectives:

- Present an overview of the standard packaging design rules.
- Study the packaging techniques available for both InP and Si-photonics.
- Present an alternative for fiber-to-chip coupling based on ball-lensed fibers.
- Describe the manufacturing process of Si-holders with v-grooves for fiber-to-chip alignment.
- Study the impact of both wire-bonding and flip-chip-techniques on electrical packaging.
- Study the behavior of ruthenium based temperature sensors as an alternative to common platinum and titanium sensors for thermal management of the system.

1.3 Structure

This thesis is organized in 6 chapters as it is presented:

- **Chapter 1: Introduction** In this first chapter the context along with the motivation are presented, as well as the structure, the objectives and the contributions.
- **Chapter 2: PIC Packaging** In this chapter a general overview on the actual Photonic Packaging techniques and design rules are presented. The Packaging process flow are also described along with the state-of-the-art technologies involved.
- **Chapter 3: Optical Packaging** In this section of the thesis a fiber-to-chip coupling technique based on custom made ball-lensed fibers is approached, including the comparison with a non-lensed fiber based technique. A brief overview on the Lithography and etching processes for fabrication of microstructures in silicon wafers is presented. The process of fabrication of Si-holders with v-grooves for fiber alignment is described in detail.
- **Chapter 4: Electrical Packaging** In this chapter a brief approach regarding the wire-bonding and flip-chip techniques is done.

- **Chapter 5: Thermal Management** This section is devoted to present two different types of temperature sensors for thermal control of the system, the Ruthenium-based sensors and Platinum- and Titanium-based sensors. For each one the resistance evolution as a function of the temperature is measure and the results are presented.
- **Chapter 6: Conclusions and Future Work** The conclusions taken from the work carried out are presented and, at the end, future work is proposed.

1.4 Contributions

The main contributions of this work are:

- Implementation of a fiber-to-chip coupling approach based on ball-lensed fibers capable of providing better coupling efficiency.
- Implementation of a fiber alignment technique based on silicon v-grooves.
- Characterization of thermal sensor based on ruthenium.

Submission of a paper to ECOC 2017 Conference:

- Pinho, Cátia, et al. “Characterization of an InP Asymmetric Coupler”.

2 PIC Packaging

2.1 Packaging Design Rules

Packaging Design Rules (PDR) ensure a correct packaging if some considerations are followed. These PDRs are based on the state-of-the-art packaging technology used by the leading photonics companies. In terms of orientation, electrical and optical connections cannot be on the same side of the PIC, thus in order to label each edge of the PIC-die the use of a compass-coordinate system proves to be an efficient approach.

Optical connections can be placed on the East and West edges of the PIC, while the North and South edges are reserved for electrical connections as shown in Figure 1.

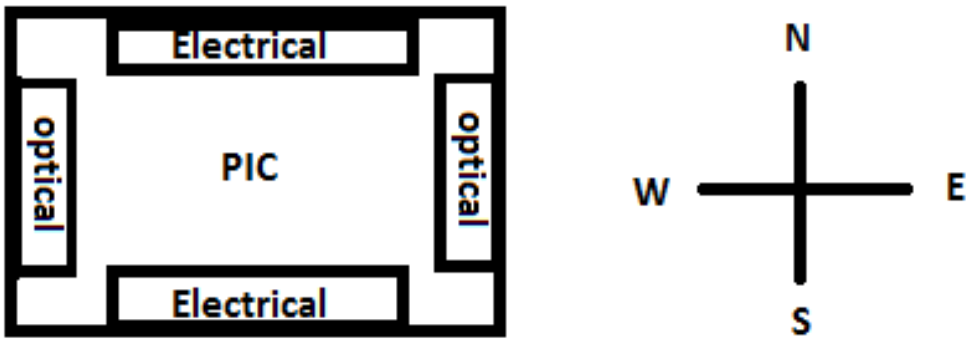

Figure 1 – Optical and Electrical Orientation.

2.2 Fiber-to-chip coupling

Fiber-to-chip coupling presents one of the major technological challenges mainly in terms of adjusting and fixation techniques, which can be divided into two fundamentally distinguishable groups: Active techniques and Passive techniques [1]. A fundamental requirement in the use of semiconductor based optoelectronic elements, such as lasers, on fiber-to-chip coupling is to ensure an efficient and reliable coupling [5-7]. This is a very important issue, because the light emerging from a typical semiconductor laser diverges rapidly as a result of its original small size, while the core of an optical fiber has a small diameter, therefore, directing the divergent light into a fiber core becomes a crucial problem [6]. The coupling between a laser source and a fiber is expressed as coupling efficiency, which is the ratio between the power coupled into the fiber, P_T, and the total power of the source, P_s [6]

$$\eta = \frac{P_T}{P_S} \tag{2.1}$$

Or coupling loss which is simply a common way of characterizing coupling efficiency expressed in dB [5]:

$$L = -10\log(\eta) \tag{2.2}$$

Two distinct approaches for fiber-to-chip coupling are considered: grating-coupling and edge-coupling.

2.2.1 Active Adjusting Techniques

The active adjusting techniques use the ability to control the adjustment under real electrical excitation conditions of OEICs [1].

In the active alignment technique, fiber-to-chip alignment is based on the maximization of coupled power [7], and the mechanically active coupling is performed by hand, one has to move either the fiber, the chip or both [8].

This method offers low excess loss, good loss uniformity and high yield, however the alignment procedure is extremely time consuming, labor intensive and has a relatively high cost [1,7], which makes this method a good approach for smaller quantities, but for a low-cost mass-produced photonic devices should be replaced by passive adjusting techniques [4].

2.2.2 Passive Adjusting Techniques

In the passive adjusting technique, elements are aligned using passive alignment structures or patterned alignment marks. The fiber-to-chip coupling was made by pre-alignment grooves suitable for mass production [7-8]. Passive alignment also provides a simple method for alignment of an array of optoelectronic parts in just one operation, thus permitting the amortization of the alignment process cost over many optoelectronic sub modes [9]. There are three considerable methods in this area of application such as, LIGA, Flip-Chip and chemical- or laser-etched V-grooves.

The LIGA technique provides a preform to produce optical waveguides and U-grooves for fiber alignment within one production cycle, then the waveguide core and cladding must be spun in further process steps on the chip, the fibers can then be putted into the U-grooves and are passively aligned [1, 9].

A lower packaging cost and compact size method is the flip-chip bonding technology in combination with high-precision patterned V-grooves. In this technique solder pads are placed on the two surfaces to be bonded and then each pad on one of the surfaces are covered with solder resulting in a strong bond which satisfices both mechanical and electrical requirements after the two surfaces are overlapped and the solder is melted and then cooled [10-12].

The fibers can be inserted into the V-grooves, fabricated by an anisotropic etching of silica substrate, allowing the alignment, adjustment and further the fixation, mostly by UV-hardened glue, to the integrated optical component.

A basic scheme of the flip-chip method combined with V-grooves for a SMF alignment is depicted in Figure 2.

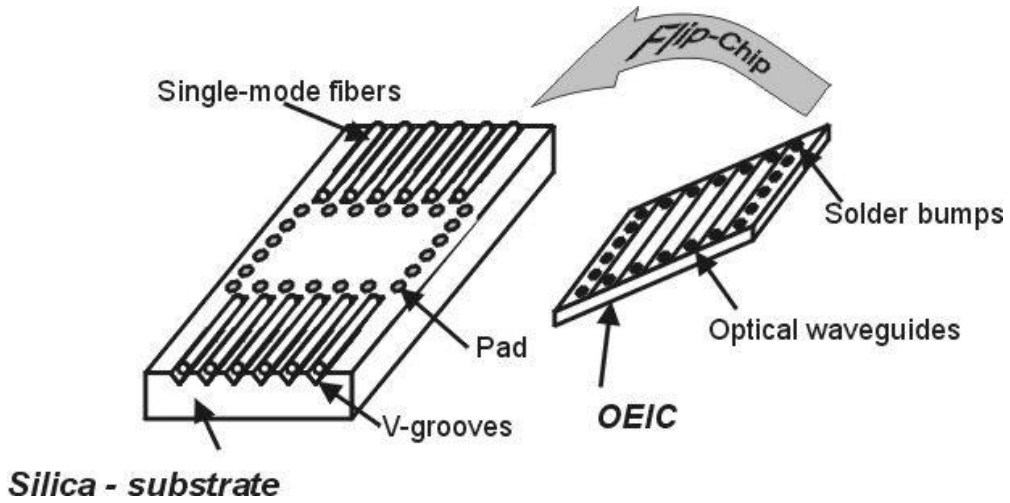

Figure 2 - Fiber-to-chip coupling with flip-chip [8].

2.2.3 Grating-coupling

A fiber-to-chip grating coupler consists of a sub-micron periodic structure lithographically etched into a high index waveguide layer [13]. Grating-coupling is a coupling technique more commonly used for Si-Photonics but it can be used also on InP-photonics however the coupler design will need to be modified at the microscopic level in order to deal with the different refractive indices and layer thicknesses of the material [14-16]. Grating-coupling are compatible with single-fiber and fiber-array coupling and in addition to offering relaxed alignment tolerances, can also be placed at any point on the PIC surface and does not require polishing of facets and allows wafer-scale testing of PICs because light can be coupled in and out of the surface of the chip [17].

Two different geometries are take into account to connect the fiber to the grating coupler: planar geometry and vertical geometry also known as pigtail geometry.

The planar geometry is recommended because it offers better mechanical stability and a lower profile packaged PIC [14-15]. For both geometries it is important to ensure that the optical-mode is incident on the grating coupler at a correct angle-of-incidence (AOI) which is typically 10 degrees for optimum coupling efficiency at the target-wavelength of the PIC design as it reduces back-reflections into the fiber.

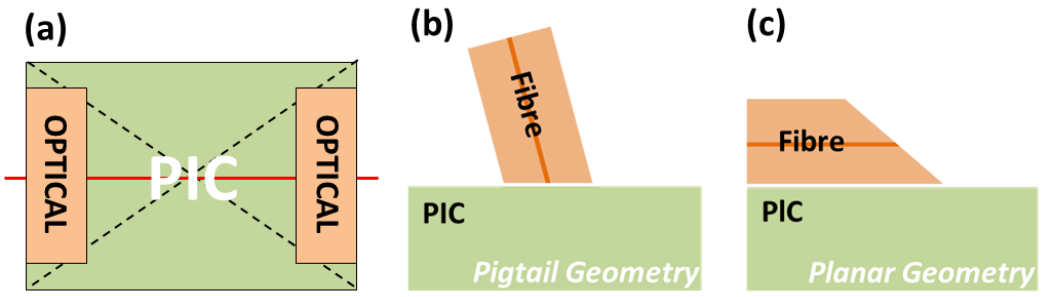

Figure 3 – (a) optical packaging orientation, (b) pigtail geometry, (c) planar geometry [13].

In order to package a fiber-array to grating-coupler array the following design rules must be followed:

1. The GC array should be arranged in straight line, parallel to the edge of the PIC-die and placed at least 0.5-1.0 mm from its edge.
2. The first and last channels of the GC array should be connected to form an optical-shunt to be used for optical alignment. – Fig.3(c)
3. The Pitch of the GC array (P_G) needs to match the fiber diameters. – Fig.3(c)
4. The GC array(s) should be centered with respect to the PIC. – Fig.2(a)

When choosing the number of fiber-channels needed for the PIC there must be used two GC channels, the first and the last one and for the optical-shunt waveguide, therefore a single active alignment of the fiber-array that maximizes the shunt transmission also aligns all the other intermediate fiber-channels with respect to their GC channels [5]. A pitch of 250 μm or 127 μm ensures that the grating-coupler array matches exactly the diameters of the fibers being used. To ensure a stable optical and mechanical-connection of the epoxy-bond it is recommended by [14-15] to have an "exclusion zone" from 0.5 to 1 mm between grating couplers and the edge of the PIC-die.

In addition, as an epoxy flow from the target region onto the main body of the PIC will occur it is highly recommended by [14-15] for the planar geometry an "exclusion zone" of 0.5 mm between grating couplers and the center of the PIC (Fig.4 (b)). For fiber-arrays in the pigtail geometry, for over-shadow typically extended from the glass end-cap of the array to the bond-pad is recommended an "exclusion zone" of 1.4 mm towards the center of the PIC-die (Fig.4(a))[13-16].

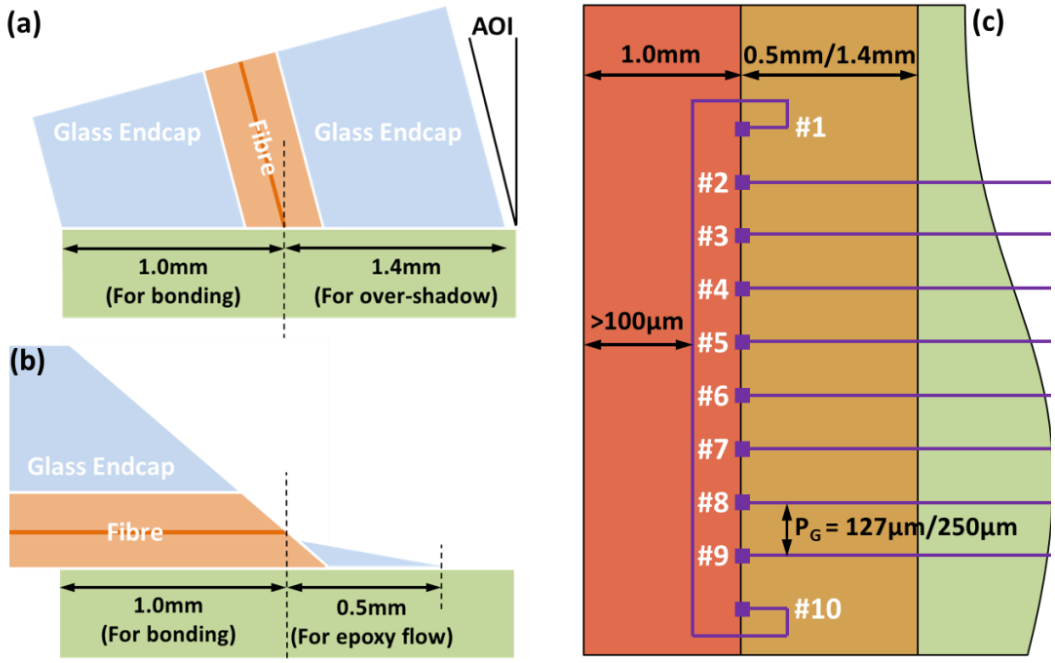

Figure 4 - (a) Side-view of a pigtail fibre-array coupled to a PIC. (b) Side-view of a planar fibre-array coupled to a PIC. (c) Schematic of a grating-coupler array with optical shunt. The top-view of the "exclusion zones" from the pigtail and planar coupling geometries are represented highlighted in red and orange [15].

Standard grating-couplers, also known as 1D grating-couplers, usually exhibit a strong polarization sensitivity, which can make them unsuitable telecom connections, due to the unknown and unstable polarization state from telecom fibers. A common solution to solve this problem is 2D grating-coupling, formed by the superposition of two orthogonally orientated 1D grating-couplers, and can accept a fiber-mode of any polarization-state, diffracting it into a pair of PIC waveguides, both TE-polarized [5].

2.2.4 Edge-coupling

Edge-coupling involves the transfer of light between the fiber and tapered waveguides located along the edge of the PIC-die, it uses lensed fibers and offers polarization-independent, lower insertion losses better than 1 dB, and broadband coupling [3,18], however when fiber array are needed it has more stringent alignment tolerances which leads to reduce the flexibility of packaging solutions making grating-coupling preferred for optically packaging PICs except for edge emitting laser chips, for example. Edge-coupling is more used in the InP-Photonics, however it could be transferred to Si-photonics [14-16] following two standard schemes explained later in this document. In order to improve coupling efficiency and pitch matching between the fiber and the input or output waveguides arrays the custom solution is the use of an optical interposer, e.g., spot size converters [5].

Edge coupling with SSC for thin waveguides usually consist of an inverse taper that gradually reduces the waveguide width far below the single mode condition in the proximity of the chip facet which an expansion of the waveguide mode profile to a point that matches the size of the laser beam in both vertical and horizontal directions, leading to high coupling efficiency [19]. For single-fiber edge-coupling, the only practical technique that can be used is active alignment of the fiber but if it is used with a lensed (to a maximum of 3 μm) or cleaved fiber (10 μm maximum) it allows fiber-to-chip coupling [14-16]. Laser welding is a very good fixation method in cases that the fiber is mounted in a metallic ferrule, because it can be locked into the perfect alignment position [14, 18], i.e., to a Kovar Butterfly-package shown in Fig.5 (a) and (b).

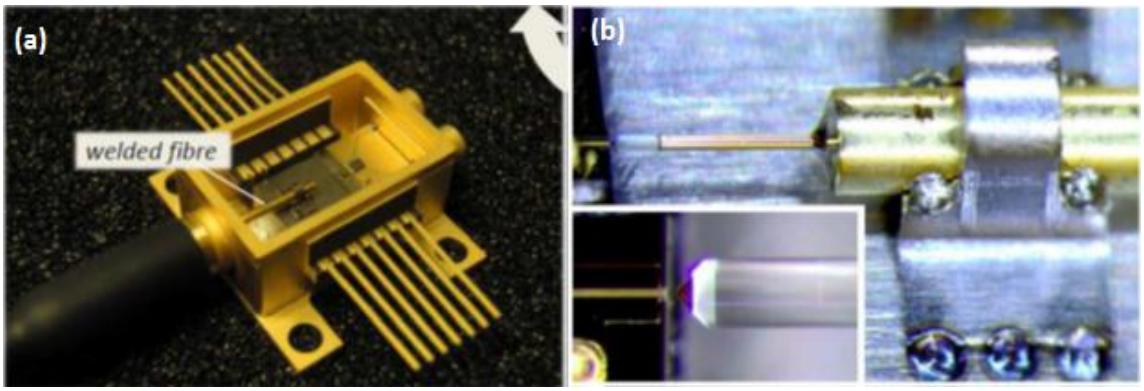

Figure 5 – Example of edge-coupling technique for photonic packaging; (a) butterfly package; (b) Microscope image of a lensed-fiber in a metal ferrule, laser-welded into perfect position [20].

For fiber-array edge-coupling it is necessary to guarantee that the individual fibers must have their cores aligned in the same direction, the array pitch must be set to 127 μm or 250 μm to match the fiber diameters and the use of lensed fiber-array is required do achieve maximum coupling efficiency.

The lack of a lensed fiber-array causes a significant reduction of the coupling efficiency to waveguides with SSC less than 10 μm. In order to limit back reflections from the coupling surfaces, a good approach is the use of angled waveguides which can be fabricated with typically 8 degrees. For coupling between these angled waveguides and fiber array, a geometric correction is need to ensure that the pitch of the waveguides perfectly matches the separation of the fibers in the fiber array.

As mentioned before, although it is more used in InP material, it can be transferred to Si-photonics following one of the two scenarios: 1-optical coupling between a standard fiber and a 10 μm mode converter on the Si-PIC; 2-Optical coupling between a lensed fiber and an inverted taper on the Si-PIC [14-16,18].

It is required that, in both cases, the inverted taper or mode converter structure is close to the edge of the PIC die for fiber access. In addition, the edge should be polished with precision, as well as post processing with polymer layers when a mode converter is used.

2.3 Electronic-IC Packaging

The packaging of electrical interconnects onto a PIC can be just as challenging as the optical packaging, this is especially the case for high-speed electrical interconnect, i.e., above 10 GHz [3]. Common approaches are monolithic integration of photonic and electronic functionalities onto a single chip and vertical integration, either flip-chip bonding of an electronic-IC (EIC) onto the PIC, or simply connecting the PIC directly to a PCB.

Standard electronic connections between the PIC and PCB are made using wire-bonding technique and to ensure a high-quality wire-bonding it is mandatory to control the location and the pitch of the bond-pads on the PIC.

To reduce induction effects, all the wire-bonds should be as short and straight as possible and staggering of bond-pads should be avoided [5,14-16].

Since optical and electronic coupling cannot be made from the same side of the PIC-die, both RF and DC square bond-pads are located on the South-side and North-side respectively by default.

For DC electrical connections, the bond-pad array should be centered with respect to the PIC and must be separated approximately 100 μm from the edge of the PIC-die, also DC bond-pads must have a side-length of 100 μm and be separated by a pitch of 200 μm (PDC) Fig.6 (d).

For RF electrical connections, the side-length of the bond-pads are also 100 μm but should be separated by a pitch (PRF) which matches the pitch of the RF lines on the PCB (PPCB) to ensure that the parallel series of wire-bonds can be drawn between the PIC and the PCB in order to reduce induction effects and the likelihood of shorting to adjacent wire-bonds [5]. Since the minimum PPCB for RF lines on the standard high-dielectric PCB is typically 300μm, it is recommended a PRF of 300 μm.

To avoid crossing wire-bonds the order of RF bond-pads on the PIC must be the same as the order of the RF lines on the PCB [14-16] this also minimize noise and induction effects Fig.6 (b).Typical layouts for co-planar high-speed single-end and differential RF lines of a standard PCB are (Ground/Signal/Ground) and (Ground/Signal (+)/Ground/Signal (-)/Ground) respectively Fig.6 (e) and (f).

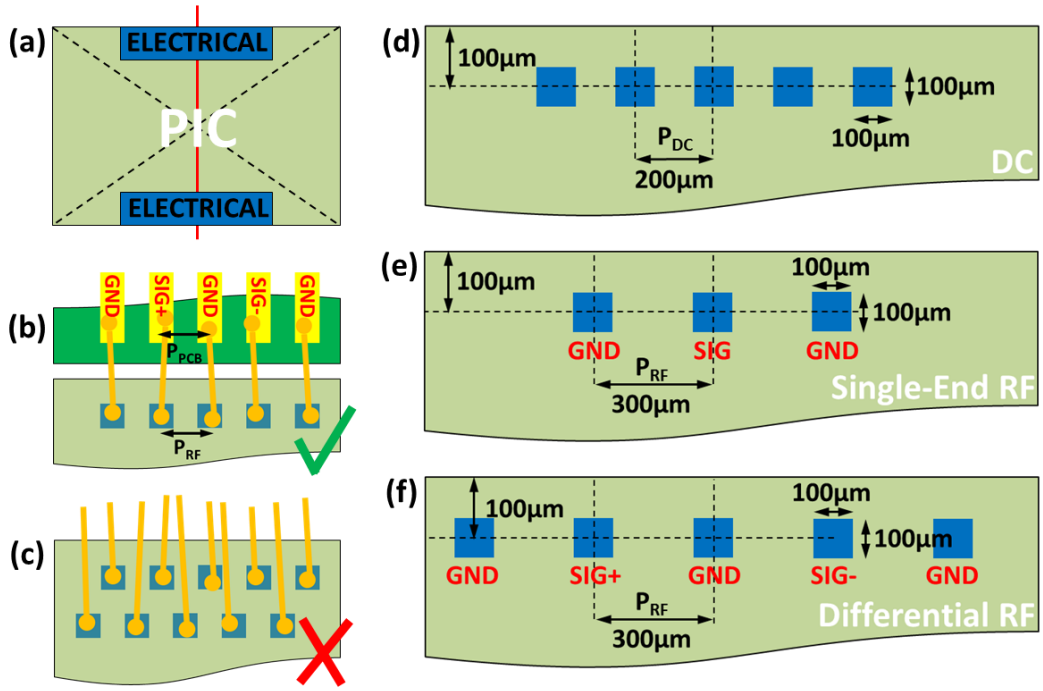

Figure 6 - Electrical connections to the PIC. (a) Bond-pad arrays centered with respect to the PIC. (b) Bond-pad spacing match the track spacing of the PCB. (c) Staggering of bond-pads must be avoided. (d) Location and dimensions of DC bond-pads. (e) RF bond-pads with single-end RF. (f) RF bond-pads with single-end RF [14-15].

The hybrid integration of an EIC onto a PIC requires flip-chip integration. Flip-chip can be made using either solder-ball-bump (SBBs) or copper-pillar-bump (CPBs) interconnects, which provide an electrical, mechanical, and thermal interface between the two chips [5,21] and improves high-speed electronic interface to the PIC as it replaces long wire-bonds with short SBB or CPB interconnects, which minimizes parasitic induction effects [3-4,22].

CPBs typically have a diameter of 20 µm to30 µm, and are formed by Cu electro-plating of the under-bump metal-pad on the PIC and EIC, followed by the deposition of a lead-free SnAgCu solder-cap [3,5], see Figure 7.

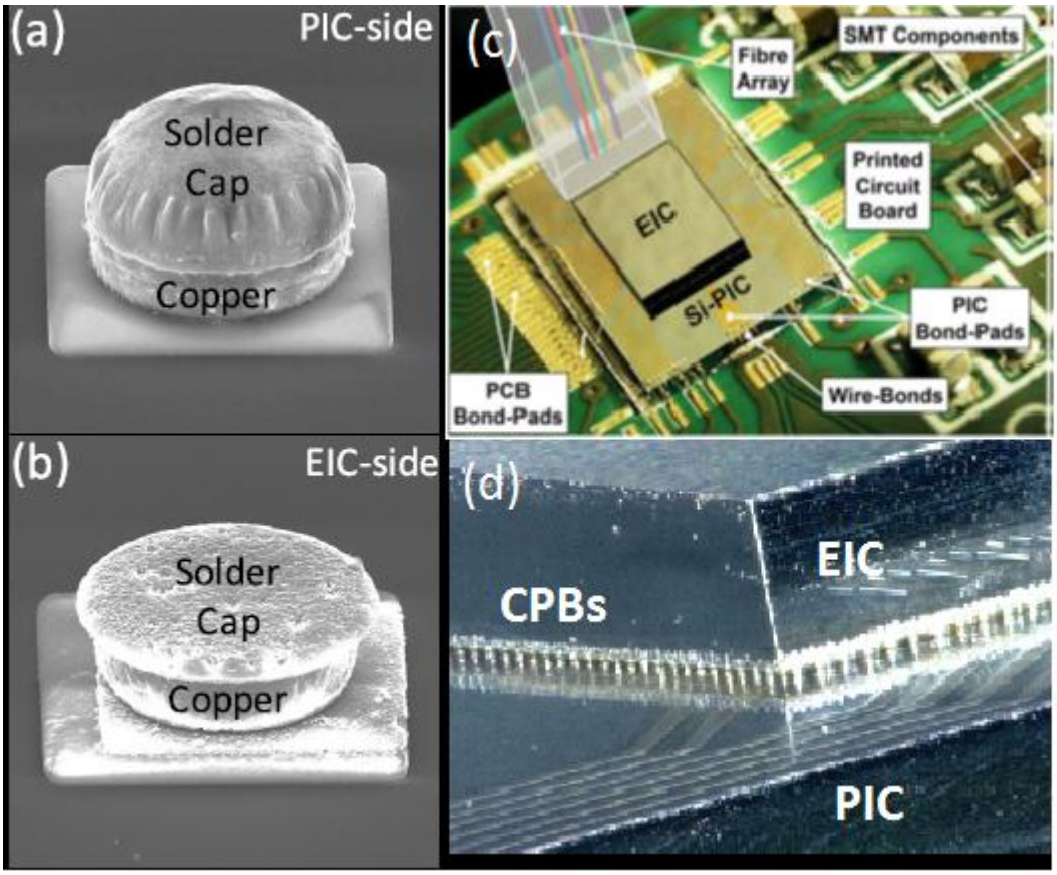

Figure 7 – Vertical integration of a EIC onto a PIC; (a,b) SEM images of the top and bottom CPBs that form the vertical interconnect between the PIC and EIC; (c)Image of an EIC integrated on a PIC; (d) Microscope image of the EIC integrated onto the PIC using several CPBs [5].

2.4 Thermal management of the module

Integrated photonic elements, such as semiconductor optical amplifiers (SOAs) and micro-ring resonators, exhibit a strong temperature-dependence that is many times greater than that of CMOS electronics [23]. A temperature variation of 20 ºC [4] is sufficient to drive a PIC outside of its operational profile.

From a practical point of view, due to the presence of thermal gradients and thermal cross-talks induced by active optical elements, heaters and electronic components, the behavior of the photonic chip may be altered compromising the stability and performance of overall system [3-4]. Furthermore, mechanical stresses induced by thermal gradients can be a problem, e.g., when fiber coupling is used.

This can be the major challenge on the PIC packaging industry, and in order to reduce and limit these behavior variations it is required to implement a thermal management system to temperature control and stabilization, the recommended is using a thermo-electric cooler (TEC), which is a solid-state heat pump that uses the Peltier effect to move heat, and a thermistor [23,24]. The added stability from the TEC allows for more efficient and better reproducibility in the local temperature-tuning of individual photonic elements on the PIC [3].

As the main objective of PIC packaging is to achieve the system better performance at a lowest cost as possible, it is important to increase the coefficient of performance (CoP) of the TEC in these modules.

It is required to use tools able to study and manage issues like thermal-stress in a multi-physical environment, and for that using COMSOL modeling [14-16] is the better approach in order to understand the transient and steady-state temperatures and thermal-gradients in packaged PICs, it helps to tune the design of the temperature sensitive integrated-components in PICs which ensures the optimum performance of the module. In practical terms, if the temperature of integrated-components exceed some operational threshold or if the PIC takes too long to stabilize the temperature after turn-on, it will be shown on thermal modeling of the PIC which is important to know when is needed to add a TEC to the packaged system improving the PIC performance [14-16].

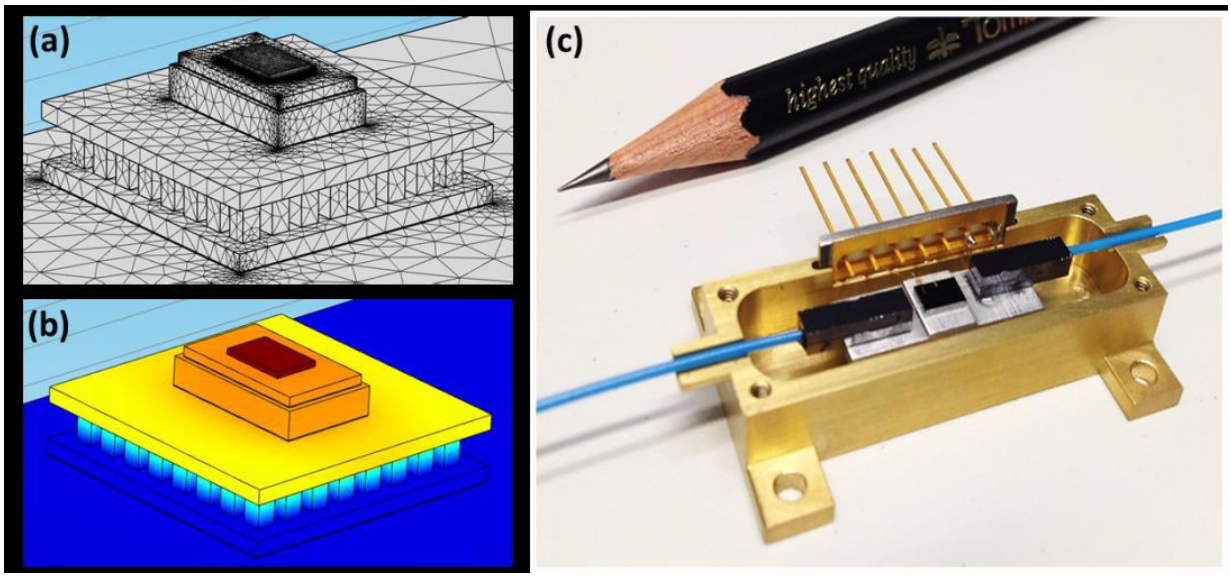

Figure 8 - (a) Physical layout of a Si-PIC, mounted onto a cooler for TEC, for a COMSOL simulation. (b) Result of a COMSOL simulation showing the thermal gradients in a packaged electronic-IC flip-chipped onto a Si-PIC. (c) Practical example of single-fiber edge-coupled to Silicon Photonic device with a custom-package for thermal control [15].

3 Optical Packaging

In this chapter some packaging of optical components techniques were studied in order to improving the optical coupling efficiency between the fiber and the chip, such as the use of lensed fibers, the impact of SSCs on the coupling efficiency and the efficient design of V-grooves for fiber alignment.

A theoretical overview of the general lithography and etching process for the fabrication of microstructures in silicon wafers is described. Then the process of manufacturing custom made V-grooves at INESC-MN clean room facilities is reported in detail.

All the procedures and conditions of measurements are detailed along with the experimental results for each technique described.

3.1 Lensed fibers

Lensed fibers are fibers with tips tapered in the form of a micro lens which is a cost-effective method for aligning the fiber to an optical device and provides highly efficient coupling [25].

Fiber tips are compact in comparison with the combination of optical fiber and discrete optical components, as they acts as lens, the effective numerical aperture of the fiber increases improving coupling efficiency [26], which turns a lensed fiber more stable and compact than a non-lensed fiber in optical coupling.

However one of the main problem with the lensed fibers is their sensitivity to alignment [6], the lens solutions always forces closer adjusting tolerances to achieve high coupling efficiencies [1]. A slight lateral movement can cause a large change in the coupling efficiency. The fiber must be brought to very close physical proximity of the laser, this has some disadvantages, for instance, if a manual alignment process is used, the fiber can touch the laser chip and cause some damages either to the laser facet or the fiber tip itself. It also becomes difficult to incorporate other optical elements such as filters, beam splitters and isolators.

Therefore the physical proximity and tight alignment requirements can make lensed fibers less attractive [6].

3.1.1 Manufacturing process of Ball Lensed Fibers

The manufacturing process of Ball lensed fibers was performed using Fujikura LAZERMaster™ LZM-100, see Figure 9, which is a glass processing and splicing system that uses a CO2 laser heat source and other advanced functionality to provide good performance, and reliability for splicing, tapering, ball lensing and other glass shaping operations on single mode fibers (SMF). By using CO2 laser fusion technology, many components with extreme geometries and critical requirements, which were very hard to make in the past, can now be easily manufactured [27].

Figure 9 – Fujikura's LAZERMaster™ LZM-100 glass processing station [27].

Before initiate the ball-lens fabrication process it was required to prepare a SMF fiber in order to fulfill the recommended specifications of the LZM-100 user guide. The first step was to strip the coating of a SMF fiber long enough so it can be held by the v-grooves of LZM-100 system with no coating, and then using the Fujikura's CT-30 cleaver the fiber was cleaved, and finally the bare part of the fiber was cleaned

with alcohol-moistened gauze. The cleaved and cleaned SMF fiber was then inserted on the LZM-100 v-groove and attached by the 250 µm holder.

Using Fiber Processing Software (FPS), a user friendly software which is a PC-based system that expands the capabilities of LZM-100, it was possible to define the essential parameters to ensure the desired Ball lensed fiber, such as the sphere diameter, the feeding speed which controls the velocity and time of the process, and the values of absolute and relative power which control the power delivered to the ball-lens fabrication process, see Figure 10.

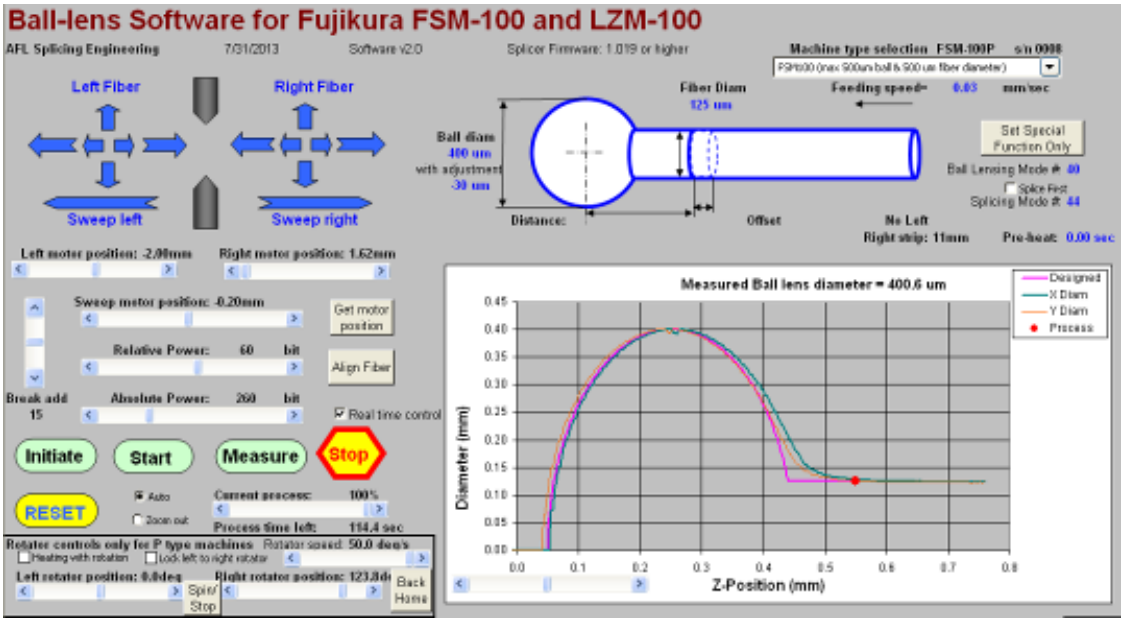

Figure 10 – Definition of the Ball lensed parameters using FPS.

By varying these parameters it was possible to find a solution to obtain the actual diameter closest to the theoretically defined. Once defined these parameters, the machine is ready to initiate the fabrication of the lenses through a heating and splicing process. Using the FPS software it was also possible to measure the actual diameter of the ball lensed produced and compare to the theoretical one, Figure 11 shows an example of real-time measurement of a theoretically defined 150 µm diameter ball lens, with default parameters, whose data was exported from FPS to an Excel file.

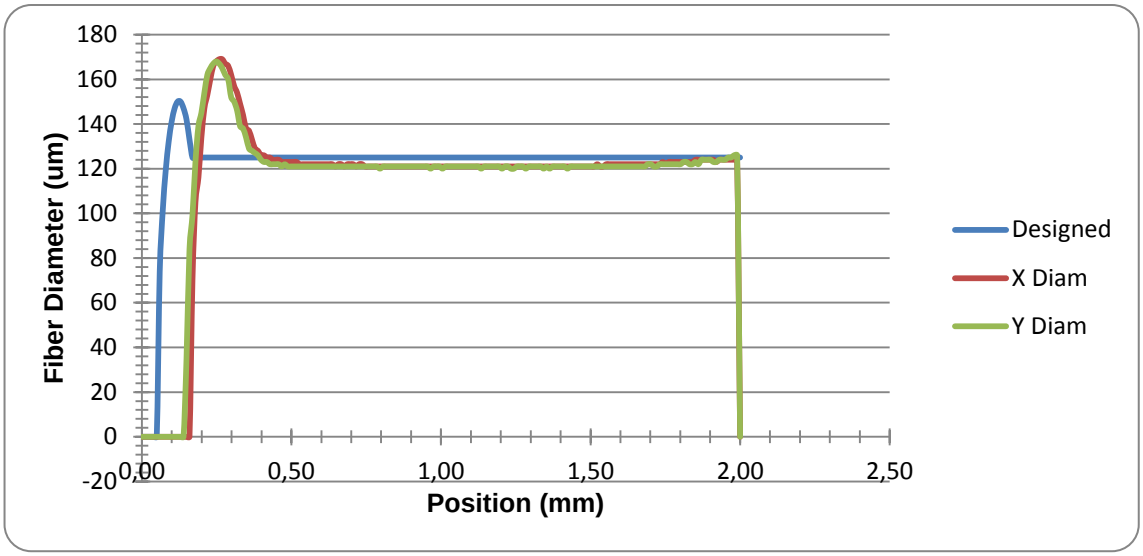

Figure 11 – Real time measurement of 150 µm Ball lens fabricated when compared to the theoretical one.

By analyzing Figure 11 one can conclude that the real-time diameter of the manufactured ball-lens is about 15 µm larger than the theoretical one, which means that to achieve the closest results as possible a fine adjustment on the parameters is required.

3.1.2 DFB Laser

Distributed Feedback (DFB) semiconductor lasers were developed during the 1980s [29] and are mainly used for WDM systems. It consists of a thin active layer between p-type and n-type cladding layers of another semiconductor with a higher bandgap. In DFB lasers the feedback is distributed throughout the cavity length, and it occurs by means of a *Bragg diffraction* which is a phenomenon that couples the waves propagating in the forward and backward directions. It is achieved through an internal one-dimensional built-in grating that leads to a periodic variation of the mode index [30,31], Figure 12 shows a DFB laser structure with the active region and the Bragg grating represented.

Mode selectivity of the DFB laser mechanism results from the *Bragg condition* [31], i.e., the coupling occurs only for wavelengths λ_B satisfying

$$\Lambda = m(\lambda_B \,/\, 2n_{eff}) \tag{3.1}$$

Where Λ is the grating period, n_{eff} is the average value of mode index, and m represents the order of Bragg diffraction. The strongest coupling between the forward and backward waves is achieved for the first-order diffraction, i.e., $m = 1$.

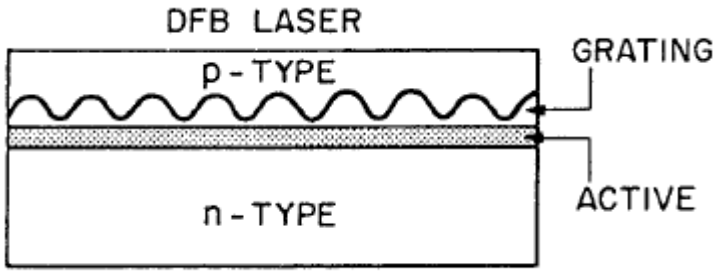

Figure 12 – DFB laser structure. The shaded area represents the active region and the wavy line represents the Bragg grating [30].

3.1.3 Testing Setup

In order to test and study the behavior of the Ball lensed fibers fabricated using LAZERMaster™ LZM-100 in terms of fiber-to-chip alignment and coupling efficiency, when compared to a non-lensed fiber, a measurement setup was mounted, as shown in Figure 13.

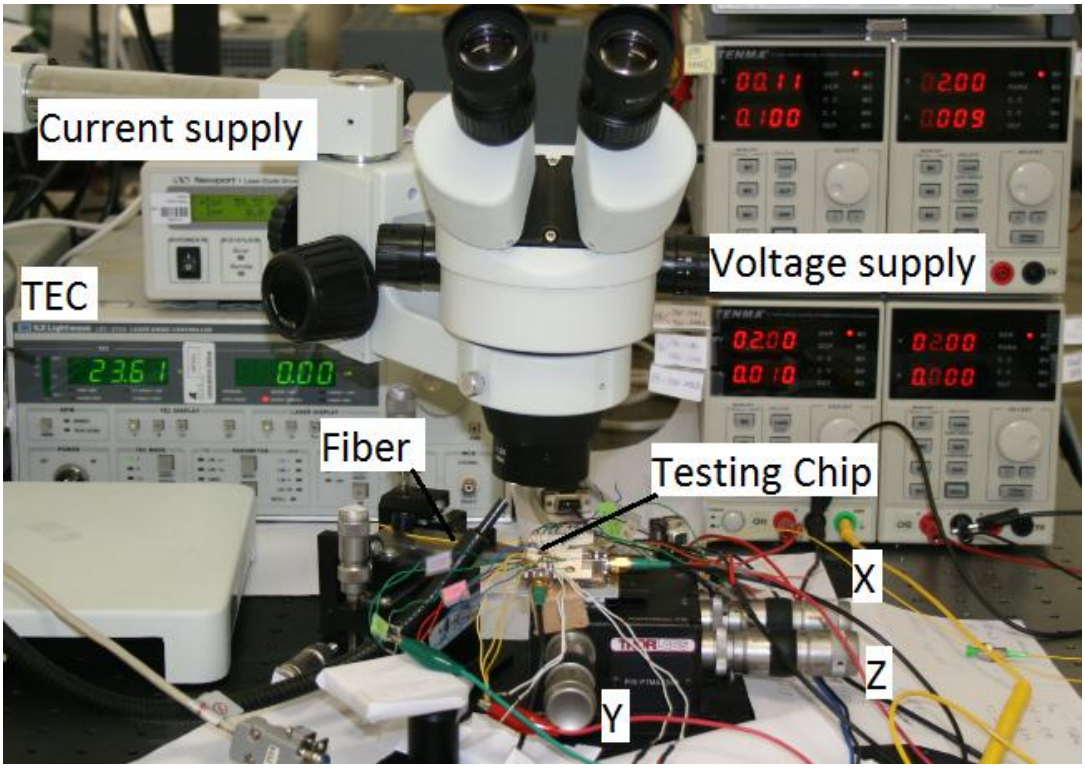

Figure 13 – Photograph of the measurement setup.

It consists on a testing chip [28], see Figure 14, placed over a peltier device with a thermistor, which is composed by one asymmetric coupler powered by two distributed feedback lasers (DFB) as optical sources, four PIN photodiodes for electrical monitoring, two phase modulators (PM), two multimode interferometers (MMI) 1x2 and two SSCs, was mounted on a three axis micro-positioning adjusting system to allow a manual coarse adjustment in the x-, y- and z-direction, a current supply to apply an input current in the DFBs lasers, a voltage supply and a PID TEC controller.

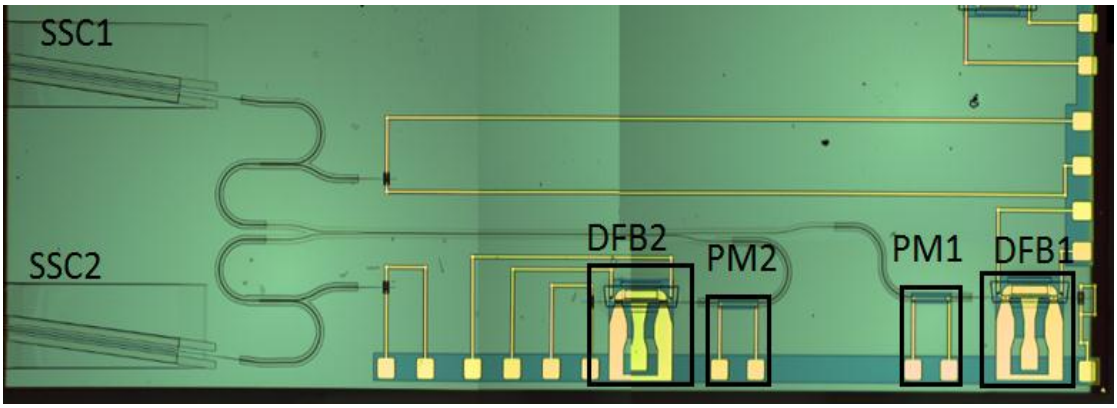

Figure 14 – Microscopic image of the testing chip [28].

3.1.4 Tests and results

Fiber-to-chip alignment was made by hand using the micro-positioners depicted in the setup presented in Figure 13, and the measures were performed followed two approaches.

Since the testing-chip is 250 μm thick, these two approaches were made with a range of ball-lensed diameters between 138 and 230 μm and a non-lensed fiber in order to prevent some damages on the lens and the chip itself.

The first one consisted on the measurement of the Maximum Optical Power received by the fiber when the laser was emitting at an input current of 100 mA, this procedure was made on both DFB laser in order to study the impact of SSC on fiber-to-chip coupling. The MOP values achieved for each ball-lensed fiber along with a non-lensed fiber was represented on Table 1.

The second one consisted on moving the fiber 2, 5, 10 and 20 μm in x-, y- and z-directions from the chip, after the MOP was achieved, and measure the optical power received in order to conclude about the impact of a slight misalignment on the coupling efficiency. For both methods the measures were taken using a power meter.

Ball-Lens diameter (µm)	SSC1 MOP (dBm)	SSC2 MOP (dBm)
0	-6,51	-7,35
138	-5,69	-6,13
167	-6,56	-7,67
180	-4,65	-5,47
200	-4,61	-5,39
230	-5,19	-5,59

Table 1 – MOP measured for each Ball-Lens diameter.

The main objective of this work was to study the improvements of the use of a lensed fiber when compared to a non-lensed fiber. By analyzing Table 1, one can conclude that the 138 and 167 µm ball-lenses does not offer significant improvements over a non-lensed fiber, it could be explained by the fact that these two samples have a small diameters when compared to the other three samples, and with a large diameter it is possible to absorb more light and consequently more power will converge to the core fiber. Therefore these two samples were discarded from the next experiments.

The following schemes show the variation of optical power measured in each fiber in response to a slight movement of the fiber from the chip in both vertical and horizontal directions. Each measure was performed at one direction at a time. Figures 15-17 illustrate these measurements performed with SSC1.

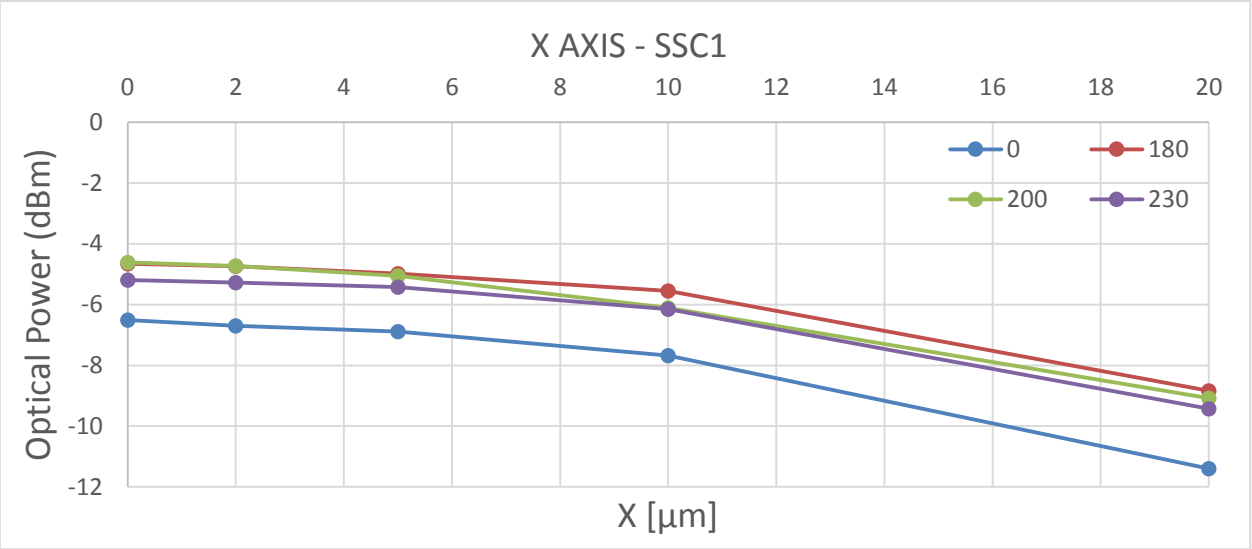

Figure 15 – Measured optical power for a 2-, 5-, 10 and 20-µm fiber misalignment in x-direction from SSC1.

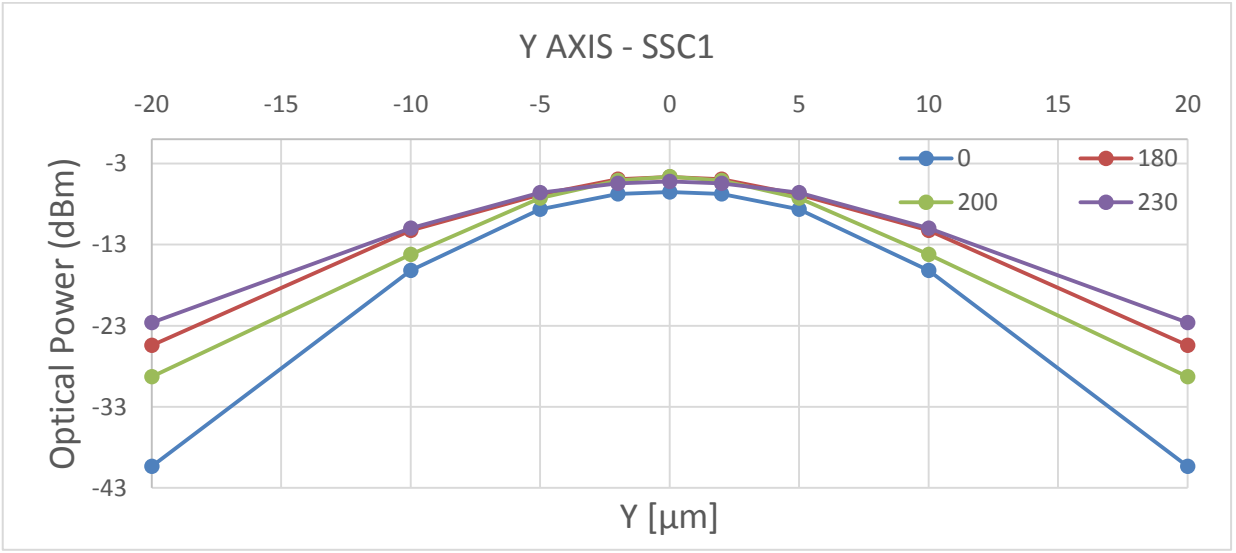

Figure 16 - Measured optical power for a 2-, 5-, 10 and 20-µm fiber misalignment in y-direction from SSC1.

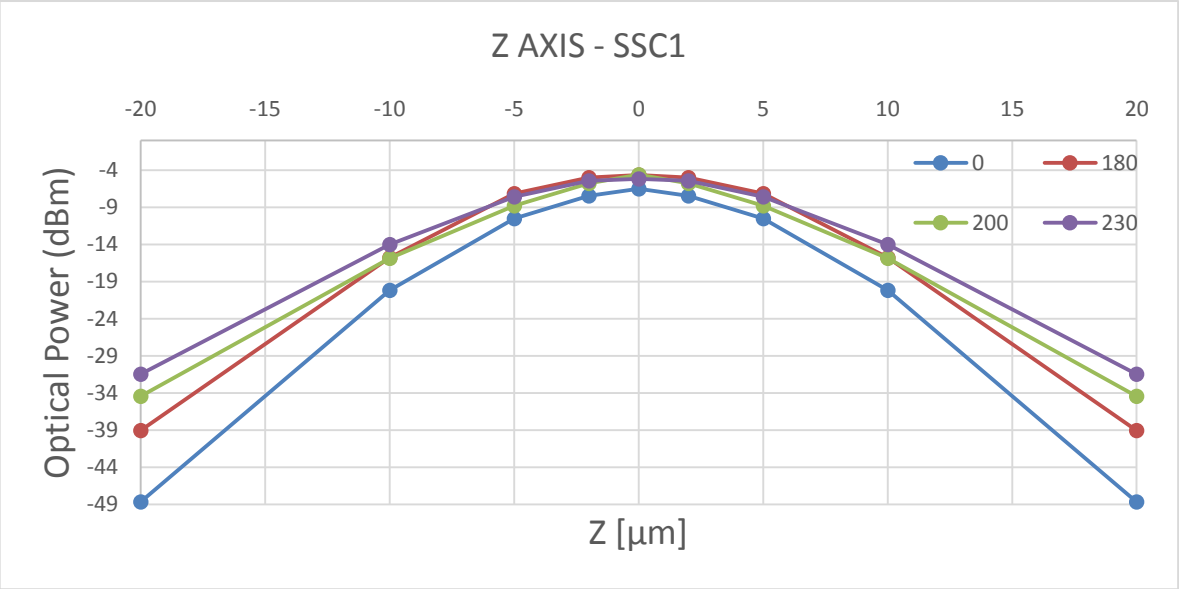

Figure 17 - Measured optical power for a 2-, 5-, 10 and 20-µm fiber misalignment in z-direction from SSC1.

Figures 18-20 illustrate the same previous tests performed with SSC2.

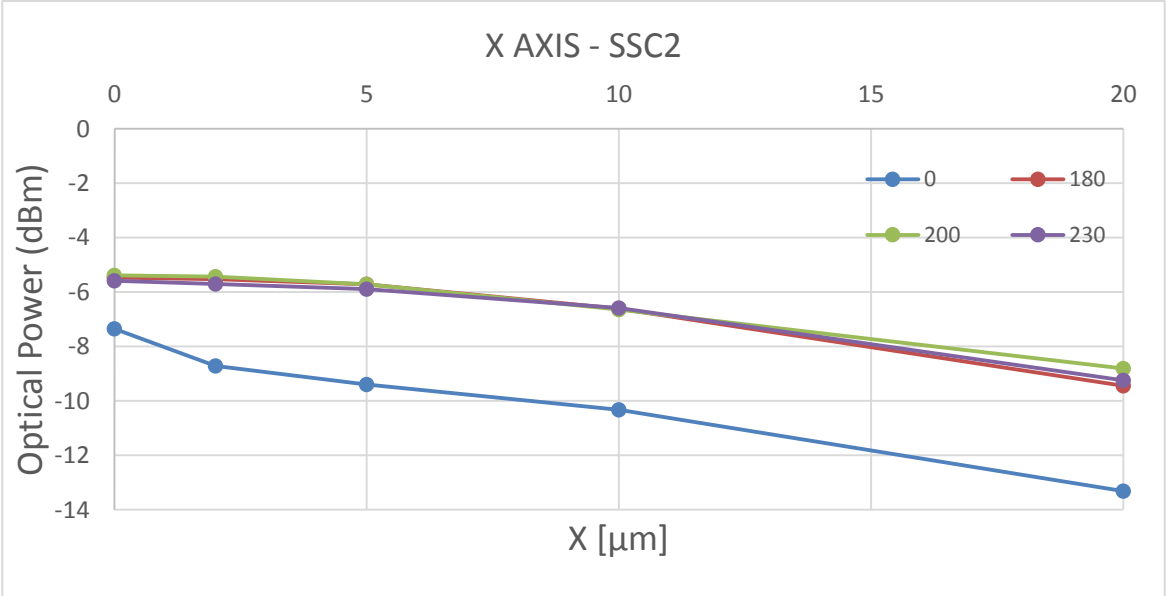

Figure 18 - Measured optical power for a 2-, 5-, 10 and 20-µm fiber misalignment in x-direction from SSC2.

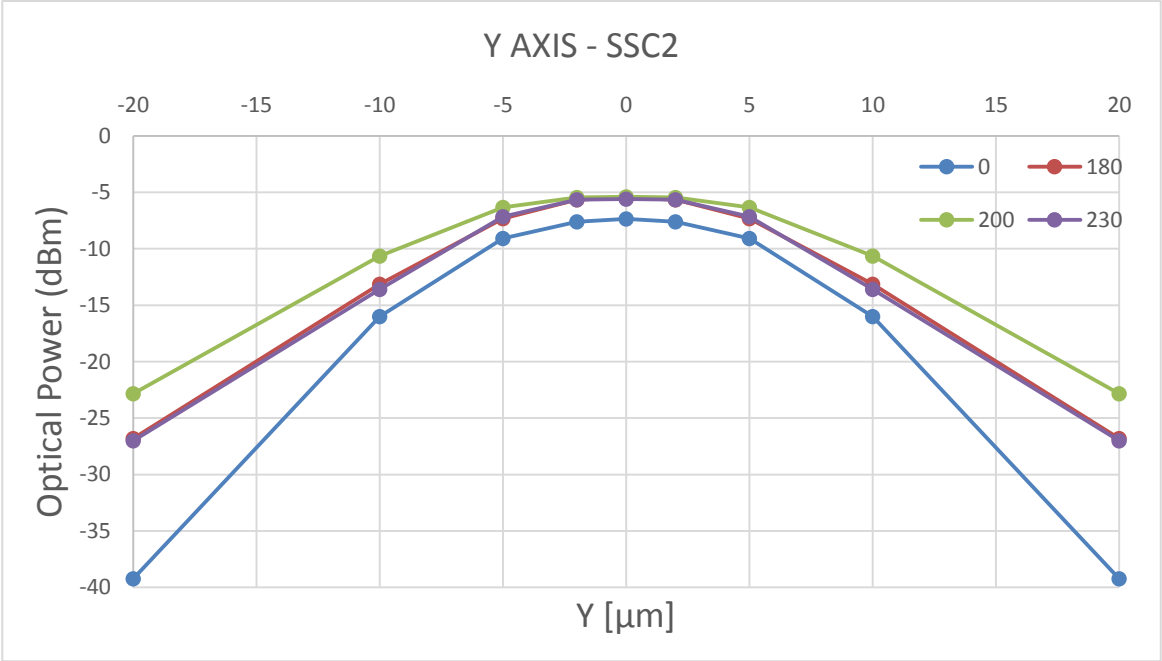

Figure 19 - Measured optical power for a 2-, 5-, 10 and 20-µm fiber misalignment in x-direction from SSC2.

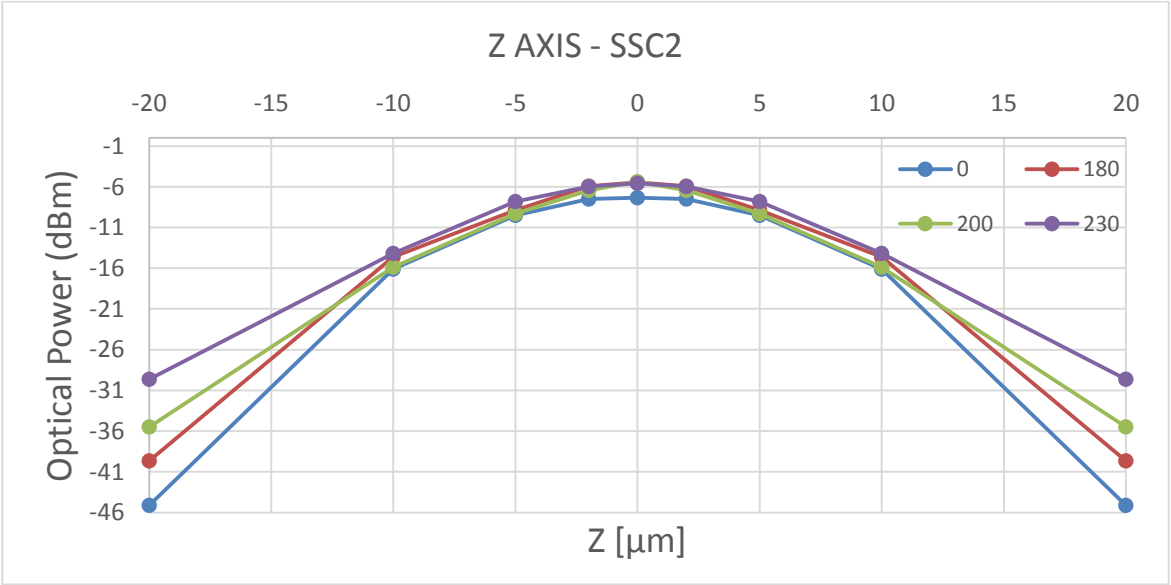

Figure 20 - Measured optical power for a 2-, 5-, 10 and 20-µm fiber misalignment in z-direction from SSC2.

By analyzing previous results, one can conclude that the 180 and 200 μm ball-lensed fibers achieved better MOP results, however they are more susceptible to a large variation of the optical power received when subjected to small misalignments. For both SSC1 and SSC2 the results are similar, i.e., bigger diameters are preferable when a movement on z-direction (vertical) is performed, due to its large diameter that allows to coupling more light into the fiber core when subjected to a vertical movement, see Figures 17 and 20. However when is applied a movement on x-direction, one can observe that as the fiber moves away from the chip, the 230 μm presents worse results. By analyzing all the results, i.e., MOP and the optical power variation when the fiber is subjected to a small misalignment, the 200 μm ball-lensed fiber proves to be the most reliable for fiber-to-chip coupling.

As mentioned before, the main objective was to conclude about the performance of a ball-lensed fiber when compare to a non-lensed fiber, therefore the use of a lensed-fiber allowed to achieve an improvement on MOP of about 2 dB, it also offers a faster and more effective fiber-to-chip active alignment and a lower optical power variation in response to a slight lateral and vertical misalignment.

3.1.5 Holder with DFB laser

In this sub-chapter it was performed a practical case-study which consists in an InP DFB laser attached to a silicon holder developed by PICAdvanced at INESC-NM. The silicon holder is composed by an etched U-groove in which the bottom is Au-plated and then is sputtered with a Sn thin-film, and two AU-plated contact pads.

The bottom of InP DFB laser was heated at 280 ˚C during approximately 10 seconds in order to melt de Sn thin-film, and then using a solder flow it was welded to the holder U-groove. Thereafter the DFB bond-pads were wire-bonded to the holder contact pads.

3.1.5.1 Testing Setup

In order to perform the tests and measures of the optical power received by the fiber a measurement setup, depicted in Figure 21, was mounted.

It consists on a thin plate with two Au bond pads wire-bonded to the holder, through which an input current is applied in the DFBs lasers, mounted over a three axis micro-positioning adjusting system to allow a manual coarse adjustment in the x-, y- and z-direction.

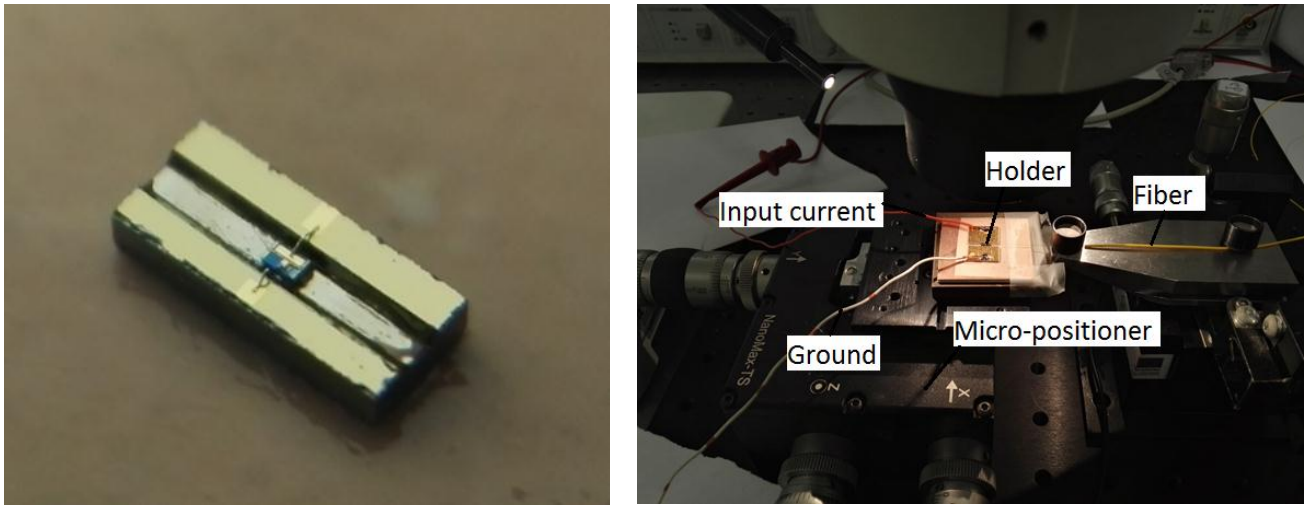

Figure 21 – Holder with DFB: Photographic image of a silicon Holder with an InP DFB laser attached (left) and a Photographic image of the testing setup (right).

3.1.5.2 Tests and Results

The tests and measures performed for this practical case-study was similar to those previously described on 3.2.4. Once again two approaches were followed. In the first one the MOP was measured with an optical power meter for each ball-lensed fiber and was compared to the one measured with a non-lensed fiber. Figure 22 shows a ball-lensed fiber directly coupled to the DFB.

In the second one was made an adjusting test by removing the fiber 20 and 50 μm from the DFB laser in order to conclude about the variation of optical power in fiber-to-laser alignment for each sample.

Both approaches were performed with an input current of 70 mA applied in the DFB laser. The measurements taken in both cases are presented in Table 2.

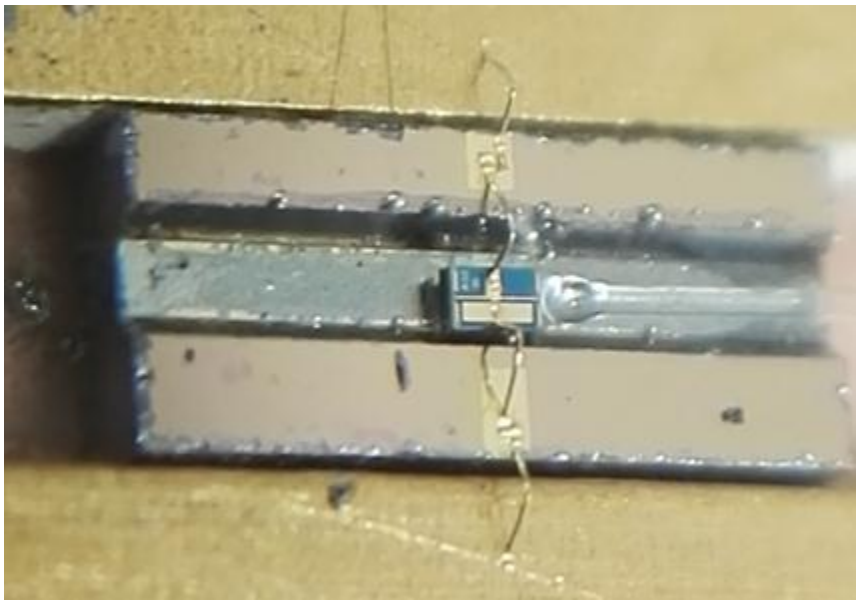

Figure 22 – Photographic image of a ball-lensed fiber directly coupled to a DFB laser

By analyzing Figure 22, one can conclude that to achieve the MOP, the fiber must be closest as possible to the DFB laser, it could be a problem as if the fiber touches the DFB it could cause some damage either to the laser facet or the fiber tip itself. Once no SSC was used, the manual alignment of the fiber to the laser has required more time and careful.

Lens diameter (µm)	MOP (dBm)	Adjusting	
		20 µm OP (dBm)	50 µm OP (dBm)
230	-2,36	-9,51	-17,16
200	-1,33	-11,8	-18,42
180	-1,14	-13,32	-21,29
0	-3,67	-13,77	-20,53

Table 2 - MOP measured for each Ball-Lens diameter and OP measured for each Ball-Lens after moving the fiber from the laser 20- and 50-µm.

By analyzing the results presented in Table 2, one can conclude that small ball-lensed diameters offer better MOP, however they have more stringent adjusting tolerances which is similar to the previous results observed for the fiber-to-chip coupling. By using ball-lensed fibers instead of a non-lensed fiber one can achieve an improvement of approximately 2 dB, it also allows for a less time consuming and efficient alignment.

3.2 Lithography and Etching

Lithography is the process of printing patterns onto a thin film usually called resist [32] the word comes from the Greek *lithos*, meaning stone, and *graphia*, meaning to write [33]. It can be divided in two different methods, optical lithography (also called photolithography) and non-optical lithography (also called electron lithography) that englobes various techniques of lithography which can be classified by the micro-tool or the type of radiation used to modify the resist layer, e. g. in photolithography the resist is called a photoresist and UV rays are used, in e-beam lithography the resist is a e-beam resist and electron beam is used, in ion-beam lithography the resist is a ion-beam resist and ion beam is used, in X Ray lithography the resist is called x ray resist and x rays are used. This document will focus on photolithography.

3.2.1 Photolithography

Photolithography was the precursor of all modern microlithographic techniques [32] and consists in a process by which patterns are formed on the surface of the wafer, e. g. is basically a photographic process by which a photoresist with a mask is exposed and developed to form 3D relief patterns on the Si substrate. It can be divided in three categories: contact printing, proximity printing and projection printing.

Contact and proximity printing are the simplest methods of exposing a photoresist through a pattern called photomask [33]. Contact printing offers high resolution once there is no gap between the mask and the wafer, however the life of the mask is reduced and can present practical problems such as mask damage which make this process unusable in most production environments. In proximity printing the mask and wafer have some gap between them, which reduces mask damage increasing the life of the mask, regarding to contact printing, however the resolution is smaller.

Projection printing is, by far, the most common method of exposure, the mask is projected onto the wafer without being in contact with it, so there is no problem of life reduction mask and the resolution is high [32,33].

The most important steps are the coating of the substrate with photoresist, the exposure to UV radiation, developing the substrate and the last one is etching with needed equipment and materials [34].

3.2.2 Photoresists

The radiation sensitive polymer, also called photoresist, is a thin layer deposited on the surface of the active material destined to receive the radiation used during the lithographic process. Photoresist is actually composed by two materials, polymer and photosensitive compound, the last one gets activated when exposed to UV radiation and then absorbs energy which is transferred to the polymer molecules. There are two types of photoresists, positive for which exposure increases the solubility and negative for which exposure reduces the solubility. Considering negative photoresist, when the polymer molecules absorb the energy from activated photosensitive compound, the molecular width of the polymer increases and it becomes more difficult to dissolve in any developer solution, so it is easy to conclude that the areas not exposed to UV light can be removed by developer solution. For the positive photoresist the process described above is exactly the opposite.

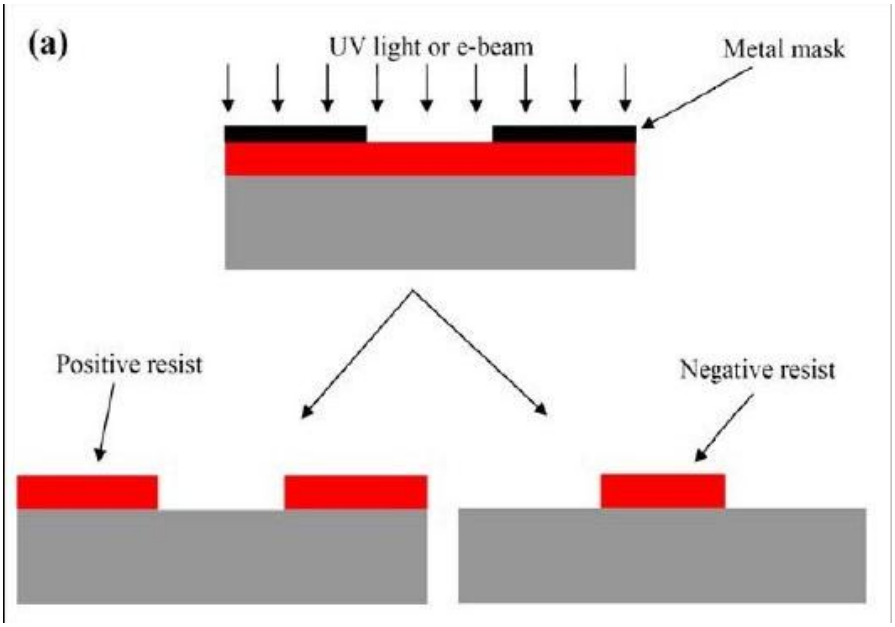

Figure 23 – Illustration of positive and negative resist after exposure and development [35].

3.2.3 Photolithography Process

There are a general sequence of steps to follow for a typical photolithography process, the first step is to coat the substrate with photoresist, the second step is to expose it to UV radiation, and then the third step is developing the substrate and the last step is Etching and strip resist with a photoresist removal. These process is depicted in Fig. 24.

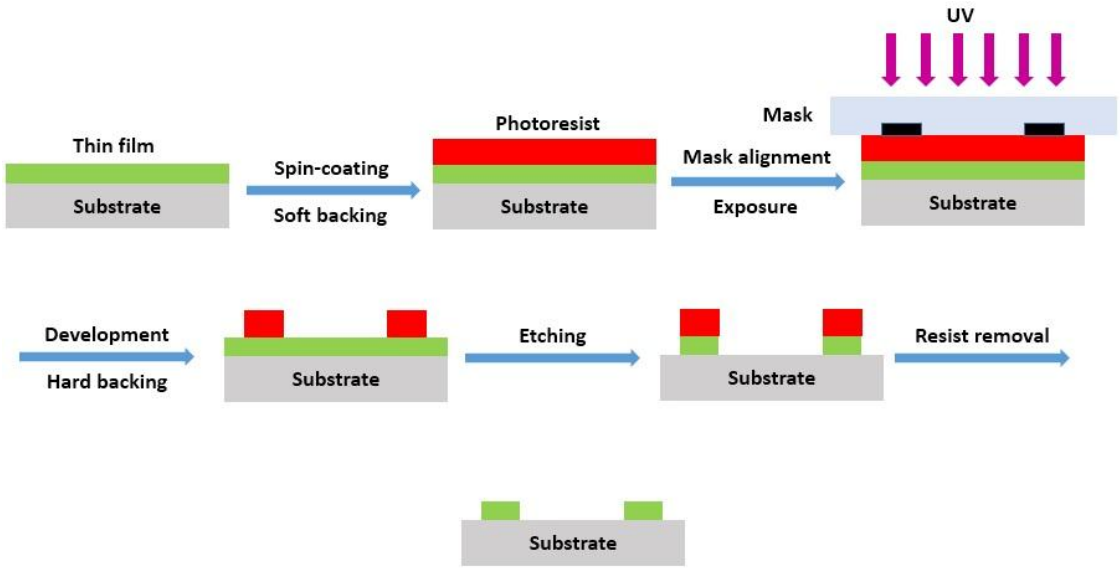

Figure 24 – Photolithography process [36].

3.2.3.1 Photoresist Coating

Photoresist coating is the first step of lithography process and it can be accomplished by a simple process of spin-coating. Initially the photoresist is dissolved in a solvent to obtained a liquid form and poured onto the silicon wafer and then it is spun on a turntable at a high speed leading to the desired film, i.e. the substrate is coated with resist. It is possible to adjust the thickness of the resist layer by varying the angular speed of the substrate on the turntable and also by adjusting the solubility of the polymer in the solvent [32]. After coating, the substrate is raised to a moderate temperature (around 100 °C) to evaporate any excess solvent, this process is called soft bake or prebake and it is used to stabilize the resist film turning thickness of the coating more uniform [33].

3.2.3.2 Alignment and Exposure

Before exposure, it is needed to bring a photomask, which is a glass plate containing information about the features to be printed, into alignment with the wafer. Considering now a positive photoresist, as it is radiation sensitive material, exposing it with UV radiation through the openings in photomask will change the properties of the exposed areas, i.e. the polymer molecules in the exposed areas of photoresist are altered by the absorption of the UV photons making them more soluble in a developing solution.

3.2.3.3 Development

After exposure, the photoresist must be developed. In the case of positive resist, immersing the substrate in the appropriate solvent removes the exposed areas of the resist leading to a formation of a hole in those regions, whereas in the case of negative resist development dissolves the resist rather in the not-exposed areas. It is important to know that the solvent does not affect the masked photoresist (as long as the wafer is not left in the solvent too long) neither affect the silicon substrate or the oxide mask.

3.2.3.4 Post-exposure bake

The post-exposure bake is used to evaporate any excess solvent molecules from the development phase and to harden the final resist in an irreversible manner by favoring cross-link reactions between the macromolecular chains [32]. In this phase, the substrate is raised to a higher temperature (around 120°C) [32,33].

3.2.3.5 Etching

The patterns printed in the photoresist layer must be then transferred to the substrate. There are three basic pattern transfer approaches: subtractive transfer (also called etching), additive transfer (selective deposition), and impurity doping (ion implantation) [33]. Etching is the most common pattern transfer approach and the idea is to use patterns printed in the resist layer to etch the sample surface solely in those areas stripped of resist after development [32] and it can be performed either using wet chemicals or more commonly in a dry plasma environment. When a material is attacked by a liquid or vapor etchant, it is removed by isotopic etching (uniformly in all directions) [37] or anisotropic etching (uniformity in vertical direction) whose differences are shown in Fig. 25.

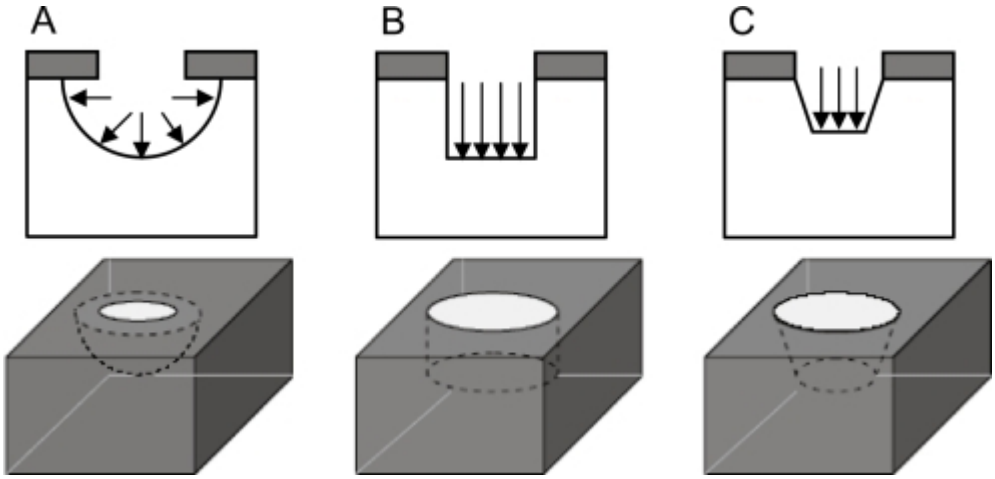

Figure 25 – Etching Processes: (A) isotropic etching, (B) anisotropic etching, (C) partially anisotropic etching [38].

➢ Wet Etching

Wet etching is a material removal process that uses liquid chemicals or etchants to remove materials from a wafer [37]. This approach has the advantages of being easy to implement, has a wide range of etching solutions for every type of material, and above all the speed of the process, which, depending on the concentration of reactive elements in the solution, can be very high (several microns per minute) [32]. However it has the disadvantage of being isotropic when nanometric patterns are needed to be etched which disallows the use of this method in the majority of cases due to undercut effects which make it difficult to control the lateral dimensions of target structures [32]. Wet etching can be distinctly anisotropic when monocrystalline materials are considered, once the etch rate can be very different for different crystallographic planes of the material. The anisotropic wet etching technique has been widely employed in the formation of silicon patterns [39]. Considering for example a solution of KOH in water, which is very anisotropic when etching crystalline silicon, this etchant solution have almost no effect on the dense planes of type {111}.

➢ Dry Etching

Dry etching method uses plasmas or etchant gasses to remove the substrate material. This method can be done using high kinetic energy of particle beams (physical dry etching), chemical reaction (chemical dry etching) or a combination of both (reactive ion etching).

Physical dry etching requires high kinetic energy (ion, photon or electron) beams to etch of the substrate atoms, there is no chemical reaction only a physical bombardment of the beams, and only the unmasked material will be removed [32].

Chemical dry etching does not use liquid chemicals or etchants, this method involves a chemical reaction between etchant gasses to attack the silicon substrate.

As mentioned before, reactive ion etching (RIE) combines both physical and chemical methods to achieve high levels of resolution [40], which today is the most widely used etch process to transfer nanometric patterns [32]. In this process one or more chemical species are used in a RF sputtering system and when these chemicals interacts with plasma, created by RF power, they will produce reactive species (both neutral radicals and ions) which can etch the substrate. Since there is a suitable balance between physical and chemical reactions, the process is much faster and achieve a highly anisotropic etch [32].

3.2.3.6 Strip

After the imaged wafer has been processed (e.g. etched) the remaining photoresist must be removed by photoresist removal solution. There are two classes of resist stripping techniques, wet stripping using organic or inorganic solutions, and dry stripping (also called plasma stripping).

3.3 Si-Holders with V-Grooves Design

The use of holders with v-grooves shows itself as the better approach to correctly align the fiber directly to the chip. Once the fiber is placed over the v-groove it can be possible to directly adjust the fiber at the perfect alignment point and desired angle to the chip.

The v-grooves must be fabricated in order that the fiber core matches the top of the substrate as shown in Figure 26.

In a partnership with INESC-MN it were designed some samples of holders with v-grooves in order to address the needs for fiber alignment for the PIC's developed by PICAdvanced. It consists of nine samples referenced by A to F, with different characteristics each, such as the number of v-grooves and the distance between them according with the respective PIC for that they were designed.

These samples were designed in two different schematics, one is for dicing at an angle of 90° and the other is for dicing at an angle of 21°, see Figure 27.

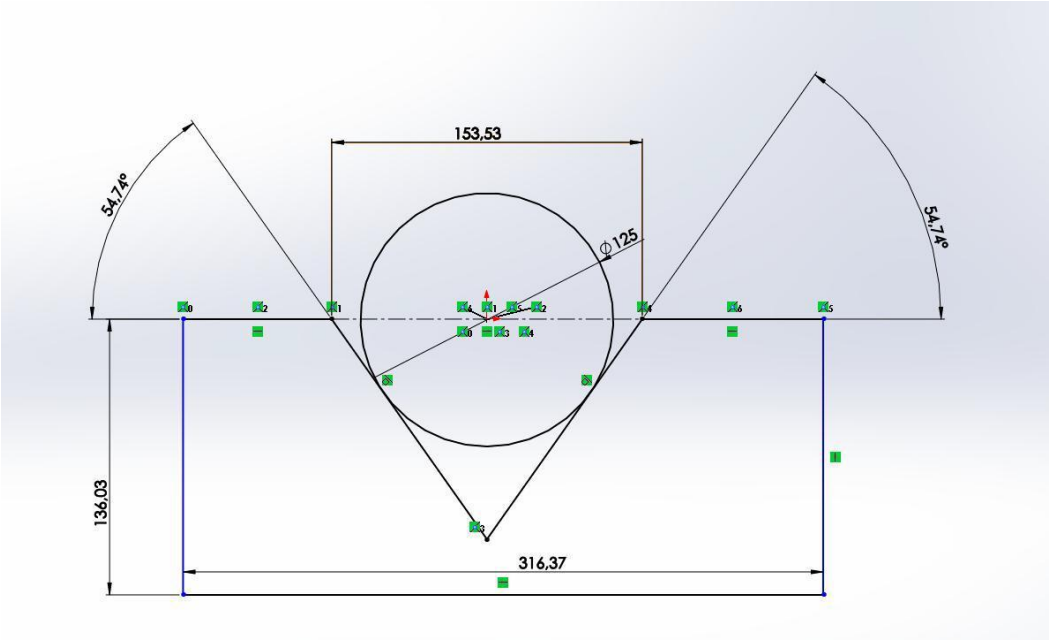

Figure 26 – Schematic with the V-groove dimensions.

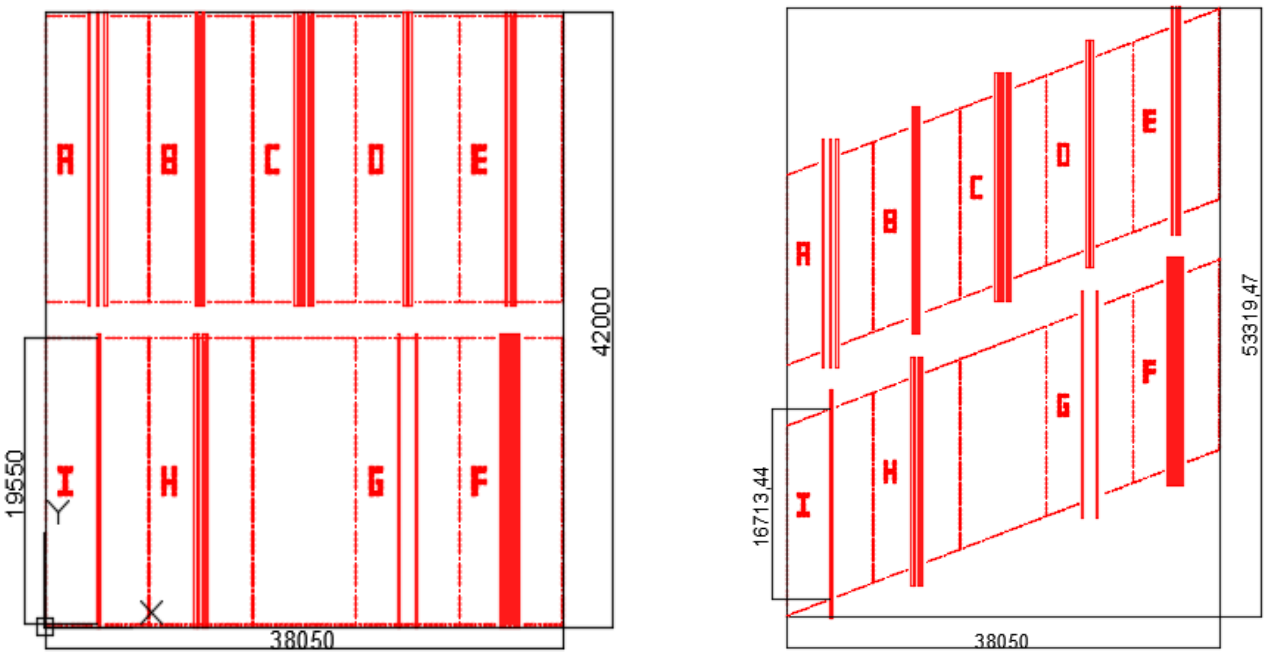

Figure 27 – Holders with V-grooves design: sample with angle of 90° (left) and sample with angle of 21° (right).

3.3.1 Manufacturing Process

The Si holders with V-grooves fabrication was performed using techniques adapted from integrated circuit manufacturing at INESC-MN clean room facilities.

The process flow follows five main tasks which are sub-divided in nine steps.

The first task consists of dicing the Si-wafer in which the samples with v-grooves are manufactured, and prepare the KOH solution for the etching step.

The second one consists of Hard Mask deposition on both sides of the wafer.

The third task consists of a pattern definition.

The last two tasks are wet etch through KOH solution and dicing the final samples, respectively.

A schematic of the overall process is depicted in Figure 28.

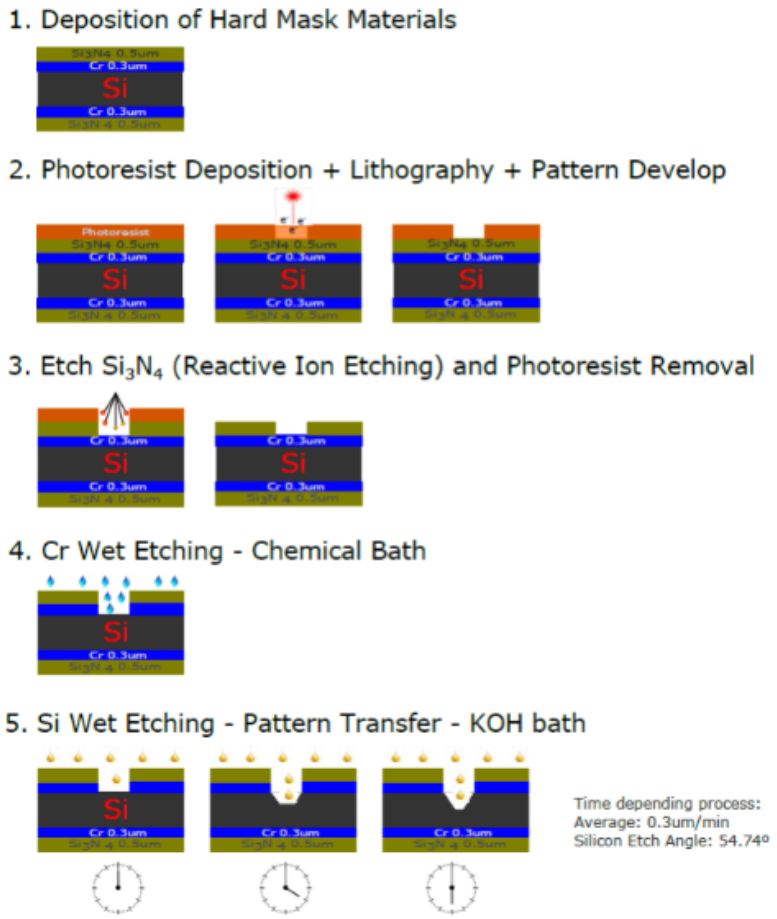

Figure 28 – Manufacturing process of Si-holders with v-grooves.

3.3.1.1 Samples Preparation

In this task the preparation of the material needed to use in process flow is performed. It consists of dicing two samples of six inches Si-wafer and prepare the KOH solution (22%) composed by 70 g KOH pellets and 190 mL of DI water, that is used for wet-etching, before the initiation of the overall fabrication process.

3.3.1.2 Hard Mask Material Deposition

This task consists of deposit of the deposition of the hard mask on both sides of the wafer and it was divided by two steps.

The first one was the deposition of a 3000 Å thick chromium (Cr) hard mask on both sides of the wafer and then the second one was the deposition of a 2500 Å thick silicon nitride (Si_3N_4) twice also on both sides of the wafer which is a protection layer.

3.3.1.3 Pattern Definition

This task is the one that englobes more steps, it consists of pattern definition and development.

Initially the samples were put in Vapor Prime for approximately 30 minutes, and then a wafer holder was cleaned on both sides so the samples were attached and fixed with Kapton tape in order to use on several machines, see Figure 29.

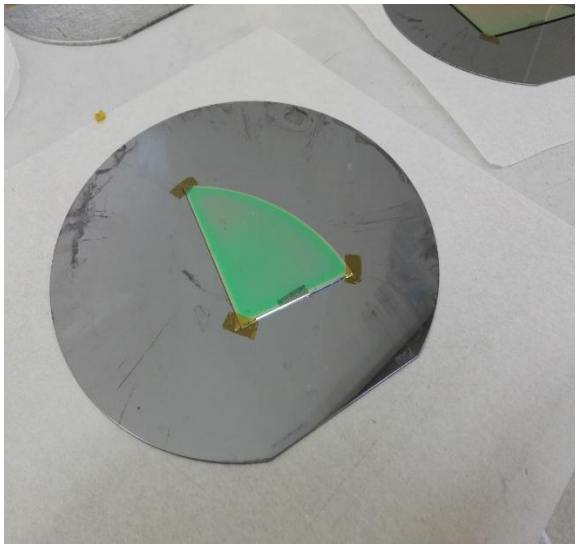

Figure 29 – Si-wafer holder with the sample attached with kapton tape.

Then using the system depicted in Figure 30 (a), the samples were submitted to a 1.5 μm photoresist deposition by a spin coating process, see Figure 30 (b) and after in order to make the resist thickness more uniform the samples were submitted to a baking process, see Figure 30 (c).

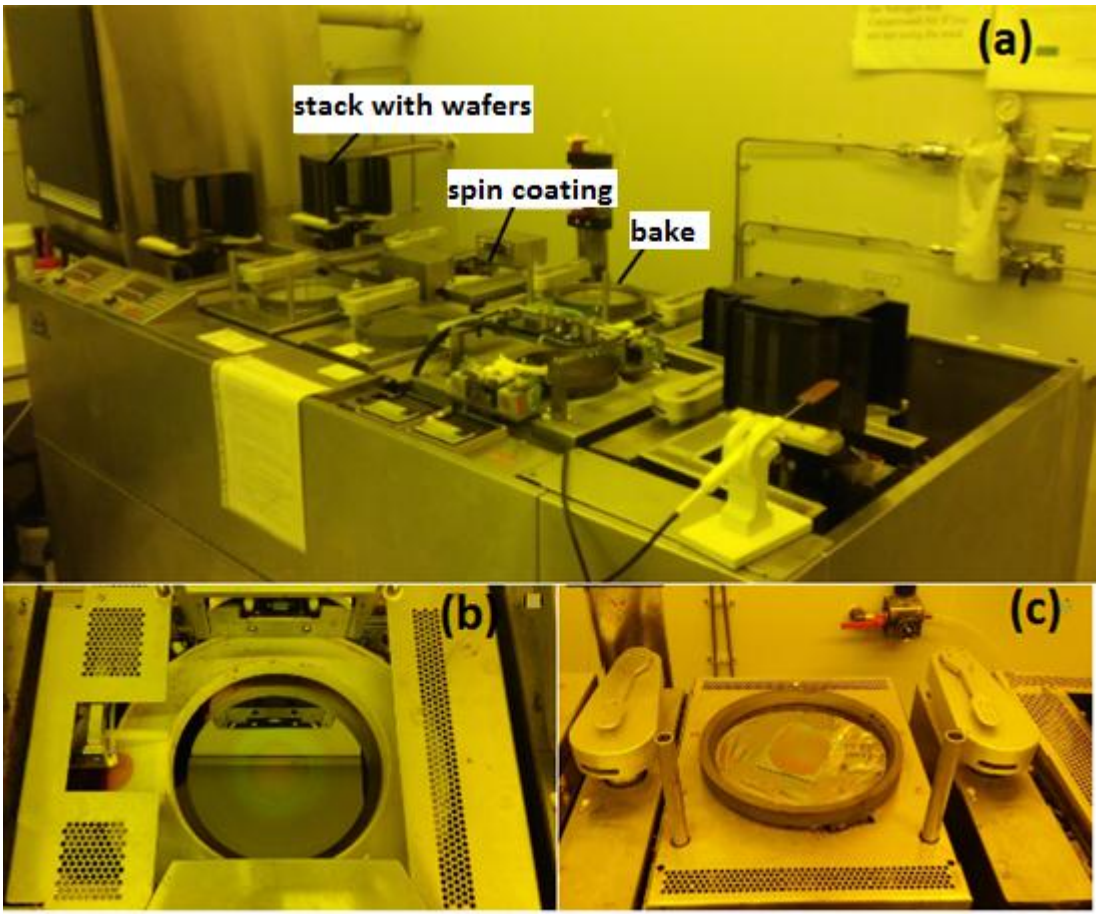

Figure 30 –Photoresist deposition process: overall system (a); spin coating (b); bake (c).

After the photoresist deposition process, the samples were submitted to a pattern definition by lithography process by laser with the DWL 2.0 Lasaray machine which works with both positive and negative photoresists, see Figure 31. In this process the 2D pattern was printed on the photoresist for further development, i.e., the e- or e+ are projected against the photoresist changing the properties of the exposed areas.

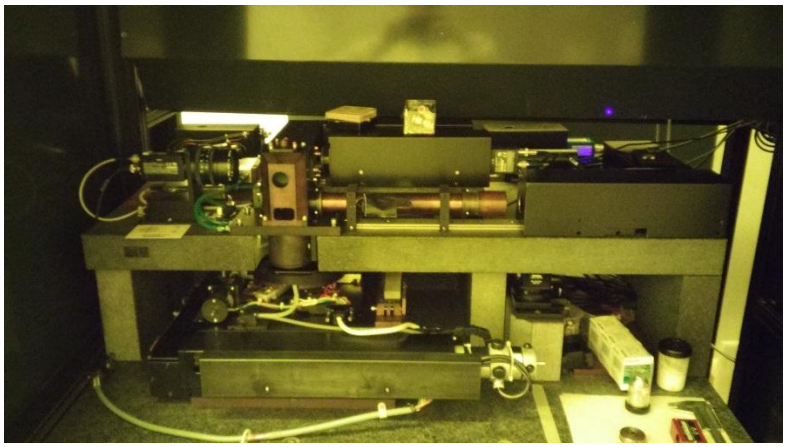

Figure 31 – DWL 2.0 – Lasaray lithography machine.

After the exposure, the pattern development was performed using the system depicted in Figure 32 (a), and it consists of a pre-bake at 110 °C followed by a quick cooling see Figure 32 (b) and then the photoresist removal with water and acetone bath by spin rinsing, see Figure 32 (c).

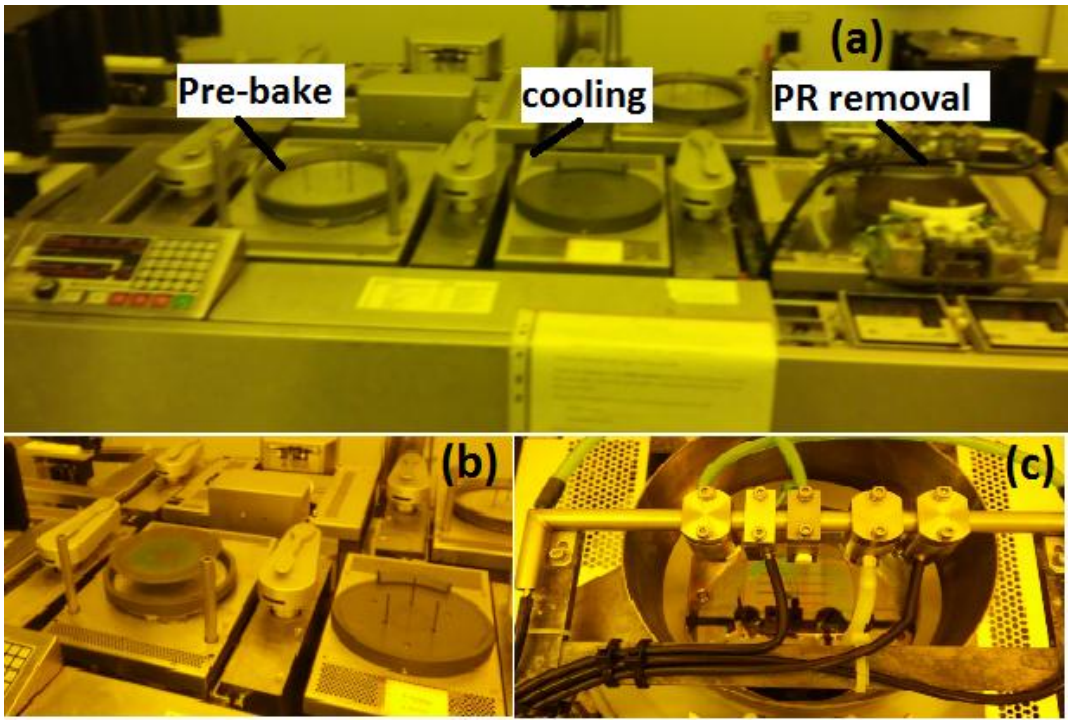

Figure 32 – Pattern Development process: overall system (a); pre-bake and cooling (b); photoresist removal (c).

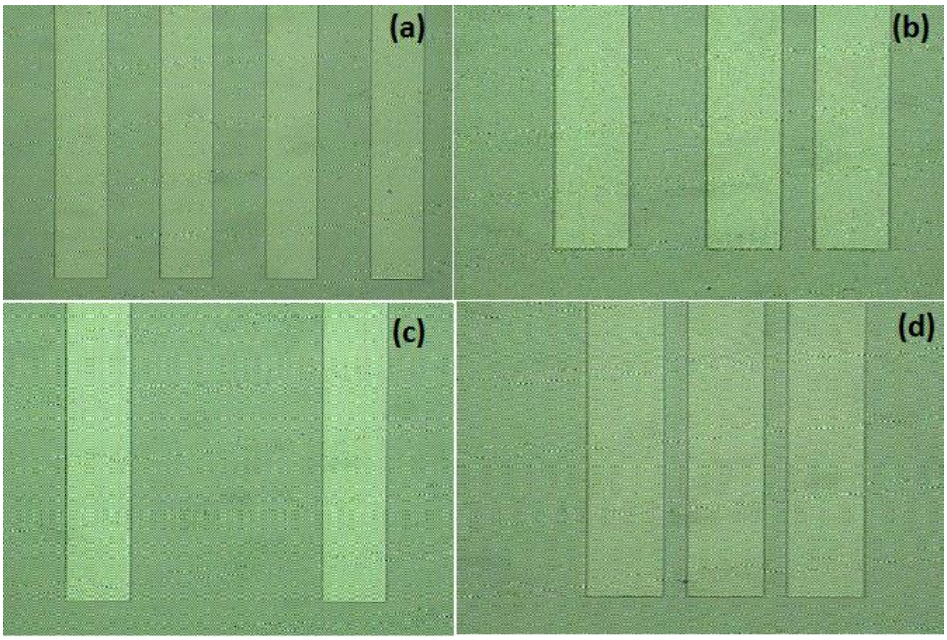

Figure 33 – Microscopic images of the different pattern samples after developing process.

By analyzing the images depicted in Figure 33, one can conclude that the exposure and development processes were done correctly because the patterned v-grooves does not present structural imperfections at this point.

The next step was the pattern transfer to Si_3N_4 by reactive ion etching performed using LAM machine, see Figure 34, in which Argon and CF4 gas were used during 1050 seconds divided by six stages of 150 seconds each to remove the Si_3N_4 protective layer of the sample. After that the remaining resist was removed with acetone, IPA and water.

Figure 34 – LAM machine.

The last step of the Pattern definition process was the pattern transfer to Cr by wet etch with Cr etchant.

The samples were placed inside a beaker filled with Cr etchant, see Figure 35, for about three minutes each and then the samples were removed and rinsed thoroughly with DI water and blow dry.

Figure 35 – Pattern transfer to Cr by wet etch.

3.3.1.4 Silicon Wet etching

In this task the sample was submitted to a wet etching with through a KOH solution (22%) prepared in advance, using the wet etch system depicted in Figure 36 (left).

The samples were placed into two plastic boxes filled with KOH solution whose quantity varies according to the sample dimensions, i.e., the sample with 6.6 cm x 8.5 cm is covered by 40 ml of KOH and the sample with 8.1 cm x 10.3 cm is covered by 60 ml of KOH solution, see Figure 36 (right), and then the boxes were placed into a glass tin filled with DI water placed on top of the hot plate. When the KOH solution reached the desire temperature of 65 °C a 7 ml of IPA was added to the 40 ml KOH solution and a 9 ml of IPA was added to the 60 ml KOH solution.

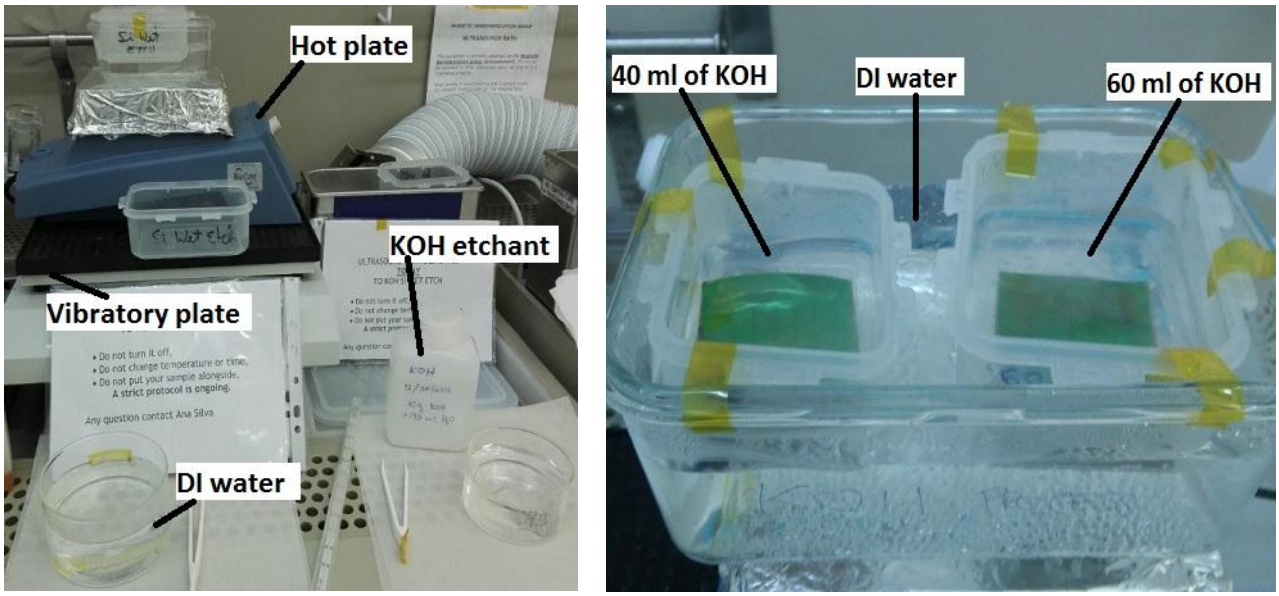

Figure 36 – Silicon wet etching through KOH solution: overall system (left) and both samples immersed in KOH solution (right).

Then the KOH solution was refilled four times with 20 ml and 40 ml in an interval of one hour during the overall etching process.

After 4 hours, the process was forced to stop because the kapton tape got loose due to the hot vapor and the containers drown in water bath.

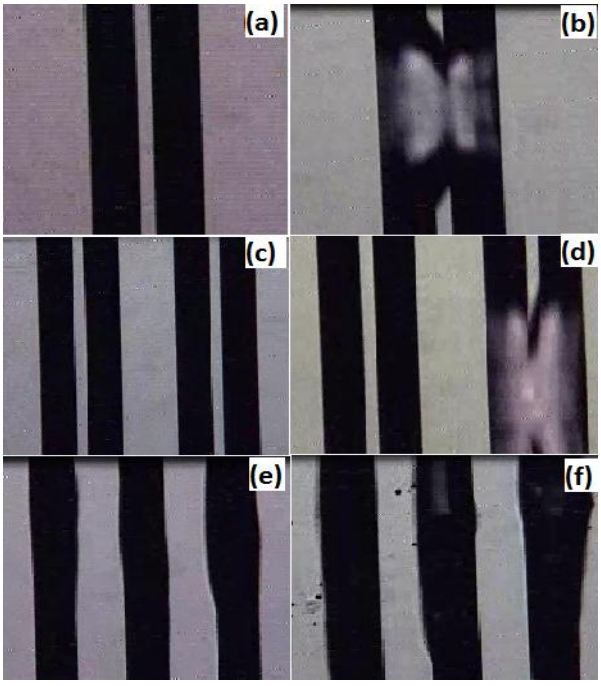

Figure 37 – Microscopic images of three holders from 21° dicing sample (left) and 90° dicing sample (right) after KOH etching.

By analyzing Figure 37, one can conclude that the represented 21º dicing samples (left) present a very well defined structure, only the sample (e) have a slightly deformation, by comparison, the 90º dicing samples represented on the right side present a poor defined structure with large deformations on each holder represented which can be explained by a possible error occurred during the lithography process and pattern design with DWL 2.0 machine, or a not properly deposition of the Cr and Si_3N_4 layers which results in a not protected area of the silicon substrate that was etched by KOH. This means that the process needs to be repeated further for the 90º dicing sample.

3.3.1.5 Dicing Process

The last task consisted of dicing both samples according to the design depicted in Figure 27, using DAD-321 dicer machine.

Two final diced Si-holders is represented in Figure 38, the 21º dicing sample on the left and the 91º dicing sample on the right.

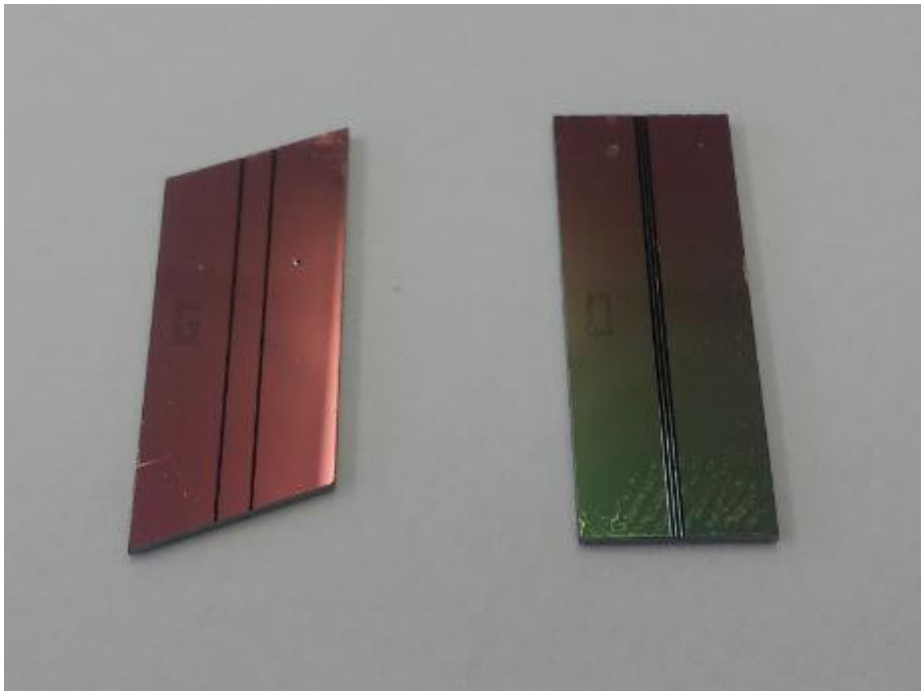

Figure 38 – Photograph of two Si-holders: 21° dicing sample (left) and 90° dicing sample (right).

4 Electrical Packaging

In this chapter two distinct approaches for electronic connections between the EIC and PIC and between the PIC and PCB are studied, which are Wire-bonding and Flip-Chip. The pros and cons for both techniques are discussed and compared in order to find the better solution for future packaging designs.

The characterization of the S-parameters for a PIC wire-bonded onto a PCB are performed in order to observe their behavior.

The measurement setup and the experimental results are described in detail.

4.1 Wire-Bonding

Wire-bonding shows itself as one of the oldest techniques to electrically bond the semiconductor components and its packaging during semiconductor device fabrication [41], see Figure 39. It consists of a thin wire bridge made out of aluminum (Al), copper (Cu) or gold (Au) which is welded at its ends to the bonding pads of the chip and the chip carrier [42] by a combination of pressure, heat or ultrasonic energy. It is generally considered the most cost-effective [43] and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages and nowadays, if properly designed, it can be used at a frequencies above 100 GHz [44].

Nowadays, more than 90 % of the IC chips used are with wire bonds because the high-speed automatic wire-bonders actually met most of the needs of the semiconductor device to the next-level packaging interconnection [41,45].

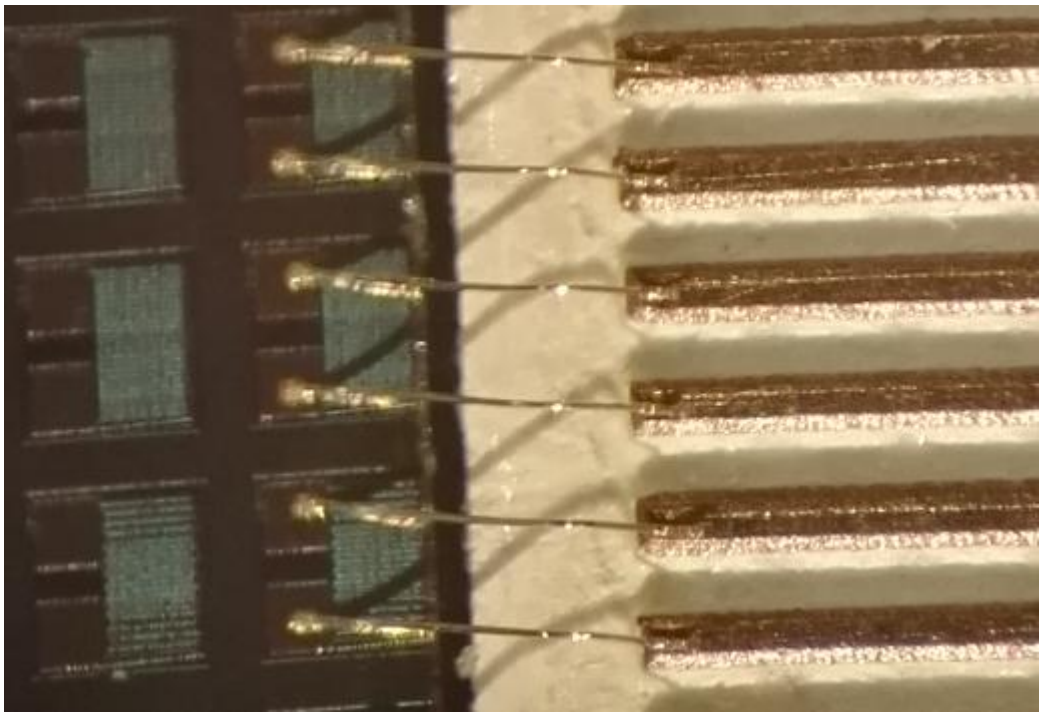

Figure 39 – Microscopic photograph of an example of Au wire-bonding.

There are two types of wire-bonds: ball-bonding and wedge-bonding, see Figure 40. Ball-bonding shows itself as a faster approach than the wedge-bonding, since it requires only three axes of movement (X,Y,Z) while wedge-bonding requires four axes of movement (X,Y,Z,θ). In ball-bonding technique only gold wire can be use once the Al wire will oxidize during the electronic flame of process to form the ball, while in wedge-bonding both Al and Au wires can be used.

By comparison, despite being slower than ball-bonding, wedge-bonding offers deep access, fine pitch, short loops and smaller pad sizes which is good for the optoelectronic and microwave application [41-46].

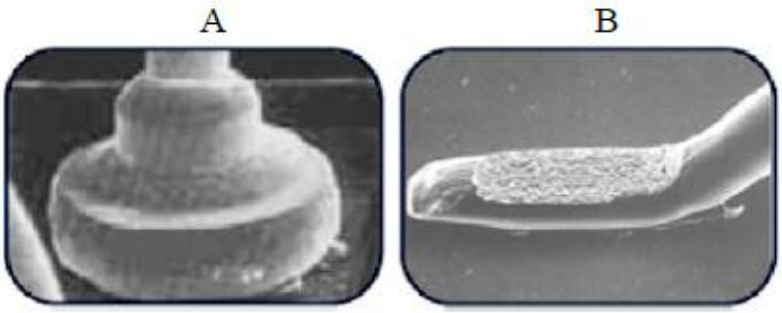

Figure 40 – Wire-bonding techniques: Ball-bonding (A) and Wedge-bonding (B) [41].

In sum, wire-bonding offers some major advantages, including a large existing infrastructure, programming flexibility, and low cost.

4.1.1 Measurement Setup

In order to measure the S-parameters the setup depicted in Figure 41 (left) was used. It consists of a testing PCB with a PIC (Figure 41 (right)) connected to a PNA-L Virtual Network Analyzer (VNA) from Agilent Technologies.

The chip , see Figure 42, is composed by an AWG filter with one optical input and three optical outputs, in which the middle output is connected to a PIN and the other two outputs are connected to an MMI with an optical output and a PIN.

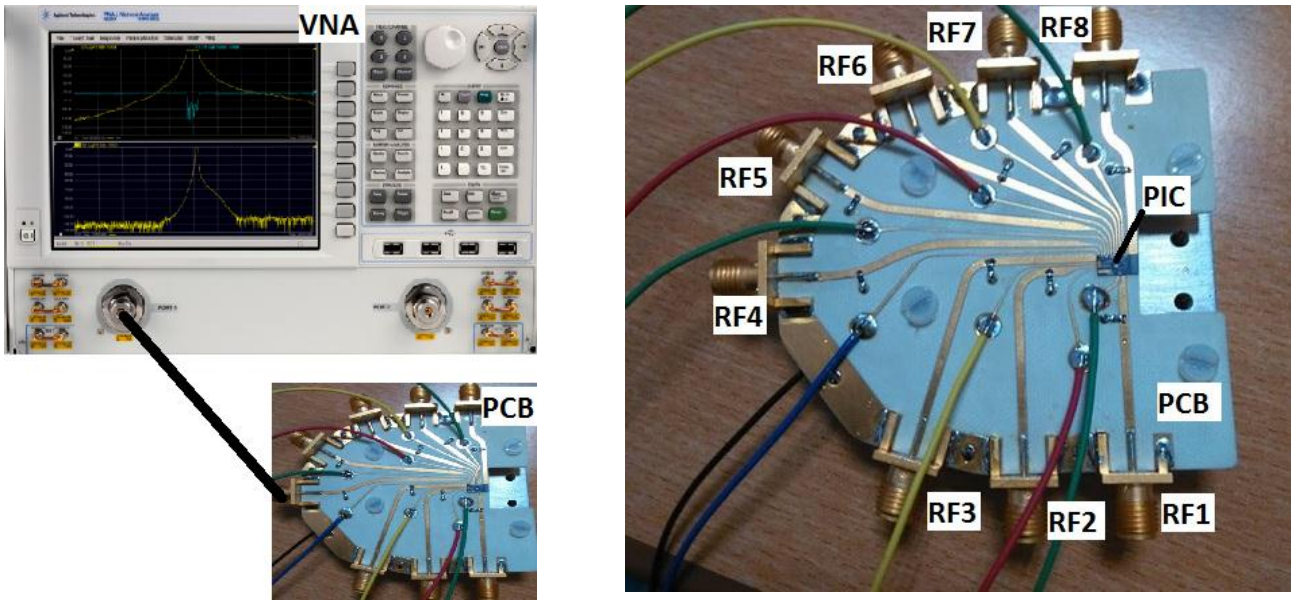

Figure 41 – Measurement Setup: overall system (left) and testing PCB with PIC and RF connectors (right).

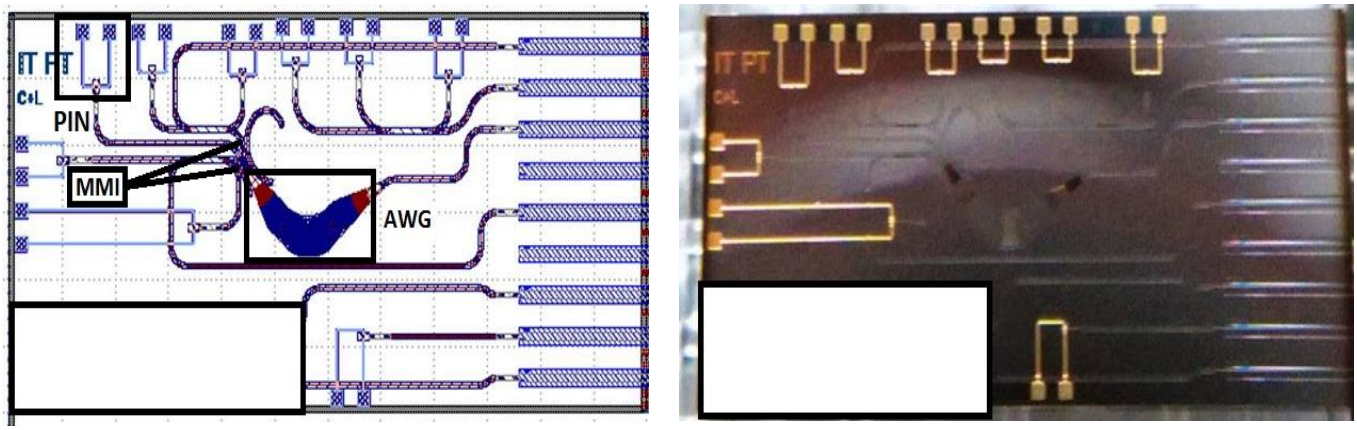

Figure 42 – Testing PIC: chip design (left) and photographic image of the chip (right).

4.1.2 S-Parameters Measurement and results

Using the setup described previously the S22 parameter was measured for all the eight PIC RF-connectors at a frequency up to 10 GHz.

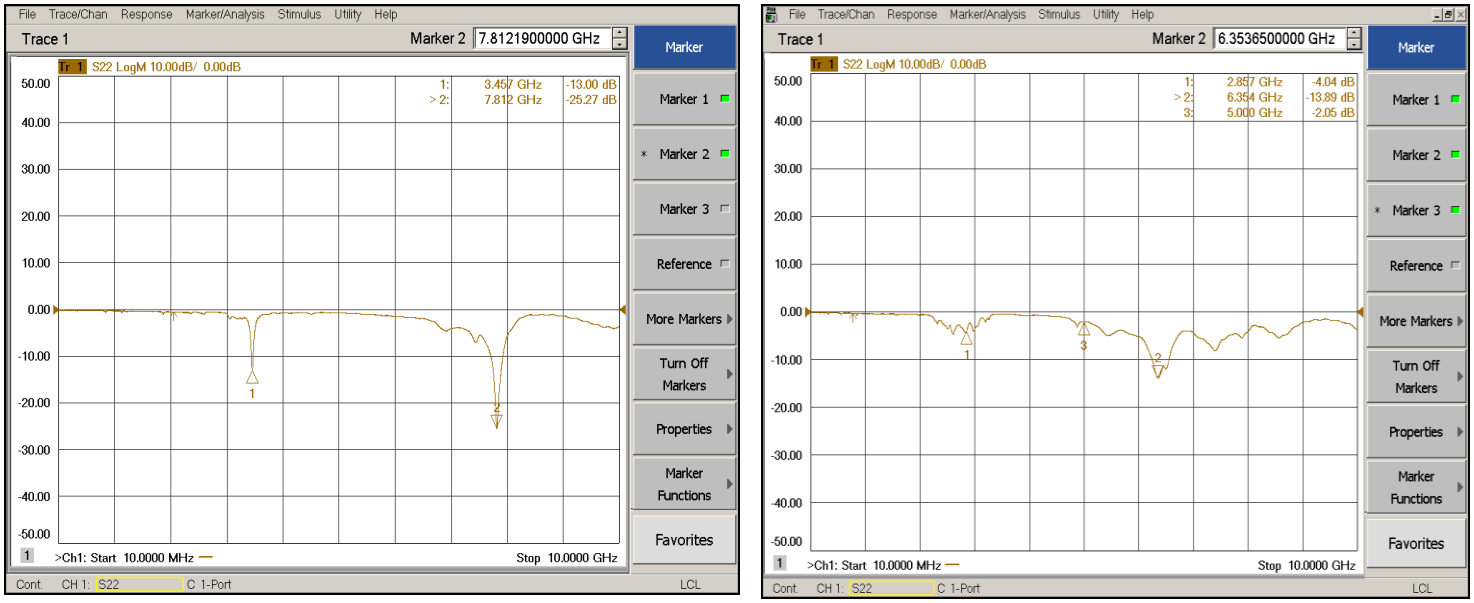

Figure 43 – S22-paremeter: RF connector 1 (left) and RF connector 2 (right).

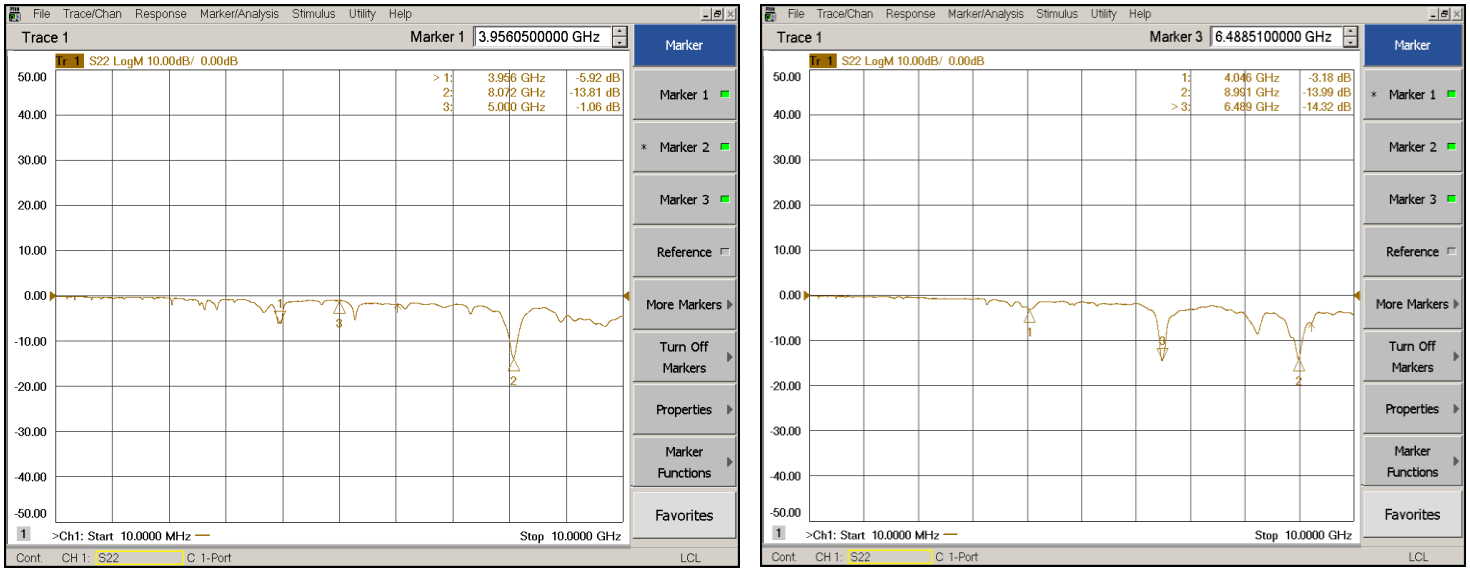

Figure 44 - S22-paremeter: RF connector 3 (left) and RF connector 4 (right).

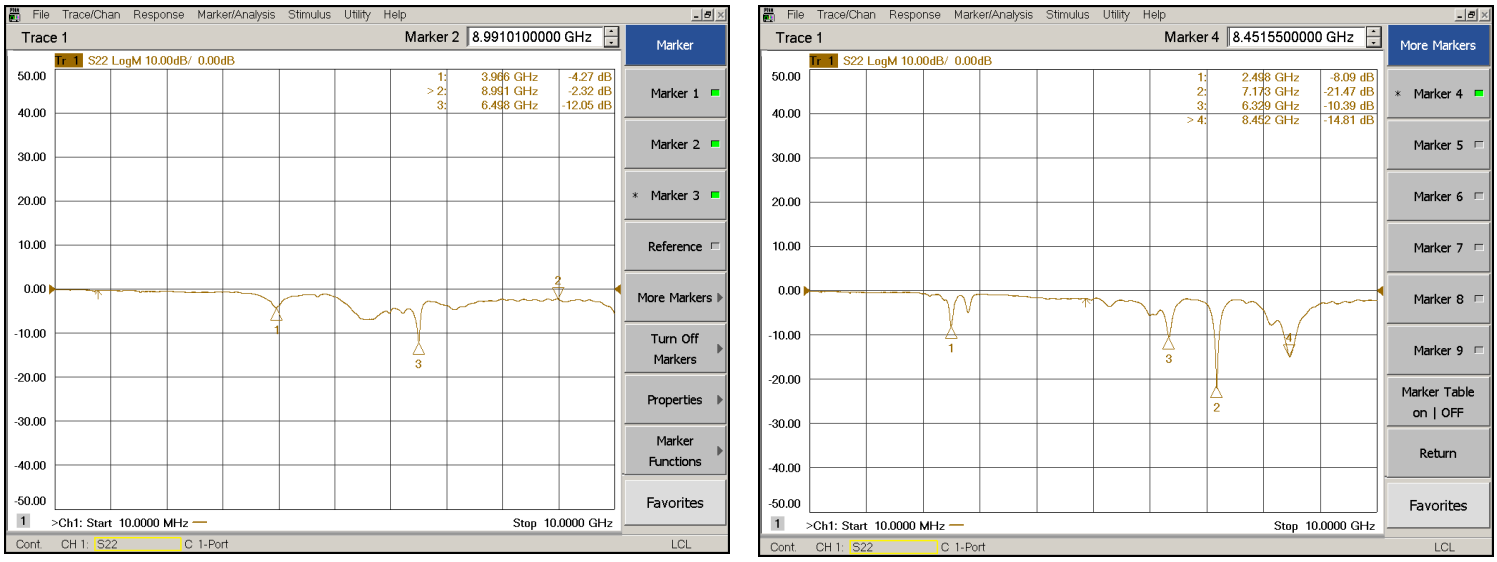

Figure 45 - S22-parameter: RF connector 5 (left) and RF connector 6 (right).

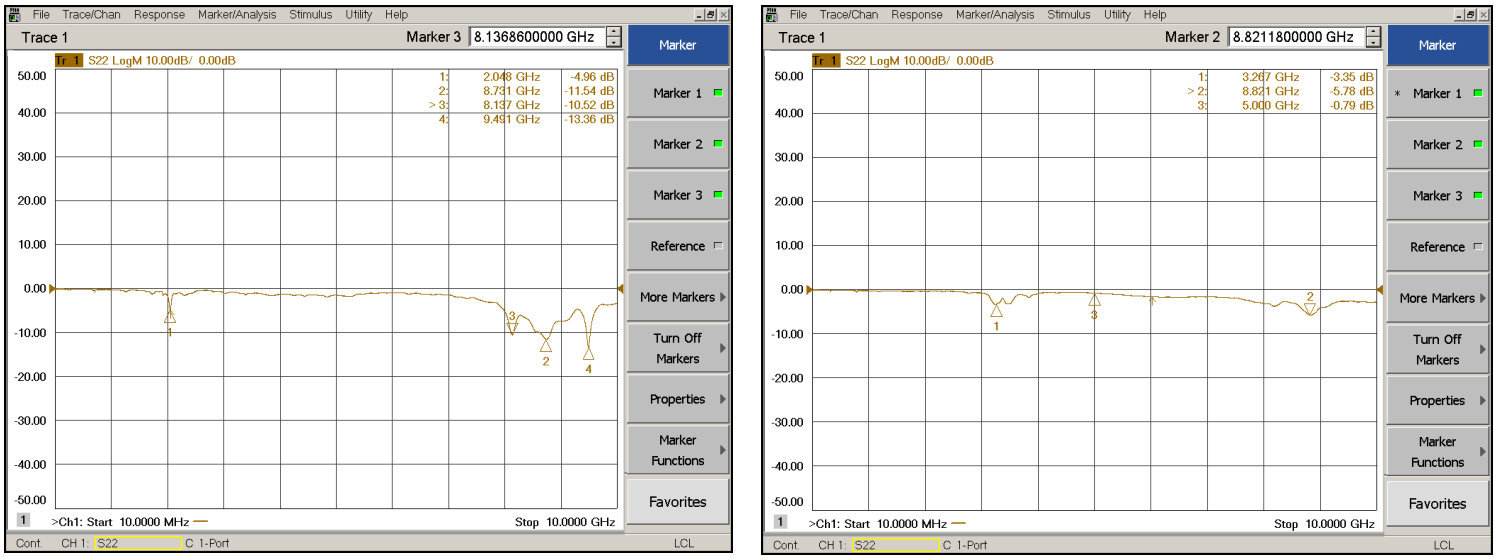

Figure 46 - S22-parameter: RF connector 7 (left) and RF connector 8 (right).

Since the measurements were made without polarization, i.e., with open circuit, the S22 parameter measures total reflection because in this case the PIN's act like a load with infinite value and the power is not delivered to the load but total reflected instead.

By analyzing the graphs depicted in Figures 43-46, one can observe that the results have some peaks which can be explained by the fact that the RF lines between the Chip and the RF connectors does not have the same width along their length which means more losses and a non-total adaptation, except the lines connected to RF1 and RF2, see Figure 41 (right), whose width is the same along their length meaning that the lines are practically adapted, thus show the better results.

4.2 Flip-Chip

In Flip-chip bonding technology the chip is attached to the package substrate using solder bumps placed over the die pads, see Figure 47 [47].

Flip-chip offers a variety of benefits when compared to traditional wire-bond packaging, including superior thermal and electrical performance, the highest I/O capability because I/O pads can be distributed all over the die not just in the borders, substrate flexibility for varying performance requirements, lower inductance due to the elimination of wires and better power/ground behavior which improves the performance [43], well-established process equipment expertise, and reduced form factors [48].

The flip-chip packaging process generally includes wafer bumping and flip-chip assembly. In the wafer bumping process, the peripheral pads on each chip in a wafer are redistributed to form area array pads. Under bump metallurgy and solder bumps are then deposited on the redistributed pads [47,49]. In the flip-chip assembly process, bumped chips, after being diced from a wafer, are placed on a substrate and undergo a subsequent reflow process [49], the underfill is then deposited to reinforce the solder bumps and enhance the reliability of the flip-chip package, see Figure 47.

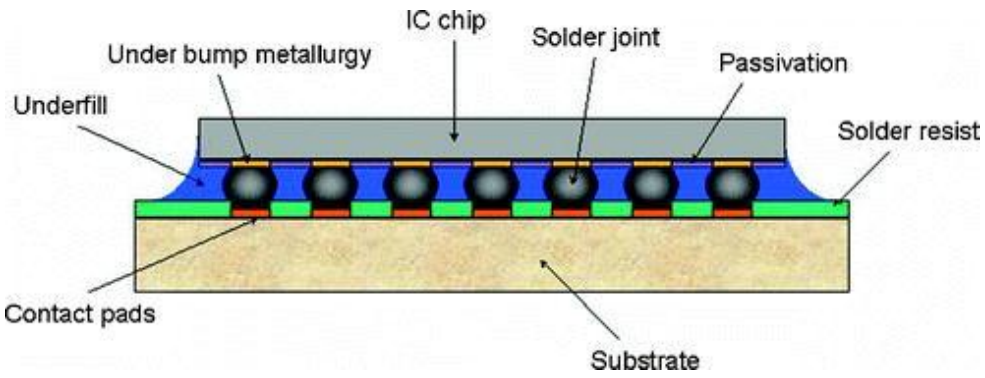

Figure 47 – Generic configuration of a Flip-Chip package [47].

Despite of the large variety of benefits described previously, flip-chip bonding technology presents some drawbacks as well, such as the mechanical stress due to different thermal expansion coefficients of the silicon and the package substrate.

5 Thermal Management

This chapter explores the study of two different types of temperature sensors, one is ruthenium-based and the other is platinum- and titanium-based sensors. It were performed measurement tests with a setup fully described, in order to evaluate de resistance evolution as a function of temperature.

All the procedures and conditions of measurements are detailed along with the experimental results for each type of temperature sensor.

5.1 Ruthenium Temperature Sensors

Ruthenium (Ru) is a hard, metallic, chemical element that is commonly found as a rare earth metal. Its atomic number and atomic weight is 44 and 101.07 $g.mol^{-1}$, respectively. It is greyish-white in color and a member of the platinum group metals (PGM) [50,51]. The use of ruthenium is emerging as its demand is rising, most is used in the electronics industry for chip resistors and water-resistant electrical contacts. In the chemical industry uses ruthenium oxide to coat the anodes of electrochemical cells for chlorine production. Ruthenium compounds can be used in solar cells and in temperature sensors. In metallurgy it is used as a hardener and alloyed with platinum and palladium.

This sub-chapter focuses on Ru-based temperature sensors, which are thin films that present low bulk resistivity and high thermal stability up to 400 ºC and have linear temperature drift sensitivity around 0.04 % $ºC^{-1}$ [52,53]. They are cheap and simpler to fabricate when compared with other thin film temperature sensors, and can be directly integrated in the electronic circuits as a thin film form. These types of sensors are being particularly used to measure and control the electrical current in spacecraft power systems [54].

5.1.1 Tests and results

The main objective in this sub-chapter is to measure the temperature dependency of resistance for Ru sensors. The tested chip consists of a 700 µm thick Si-based substrate were thin film Al heaters and u-shaped Ru thermal sensors are fabricated using techniques adapted from integrated circuit manufacturing available at INESC-MN clean room facilities [51] see Figure 48 (left). Since the bonding pads were Al based it was not possible to use wire-bonding onto a testing PCB, so in this case the tests were performed using DC-probes instead.

It was used a setup that consists in a TEC composed by a peltier device with a thermistor where the PCB with sensors is placed over, and a Temperature controller model 3240 from NEWPORT, the values of sensors Resistance were measured at their terminals with a Keithley multimeter from Tektronix Company with a circulating DC current of 1mA, see Figure 48 (right).

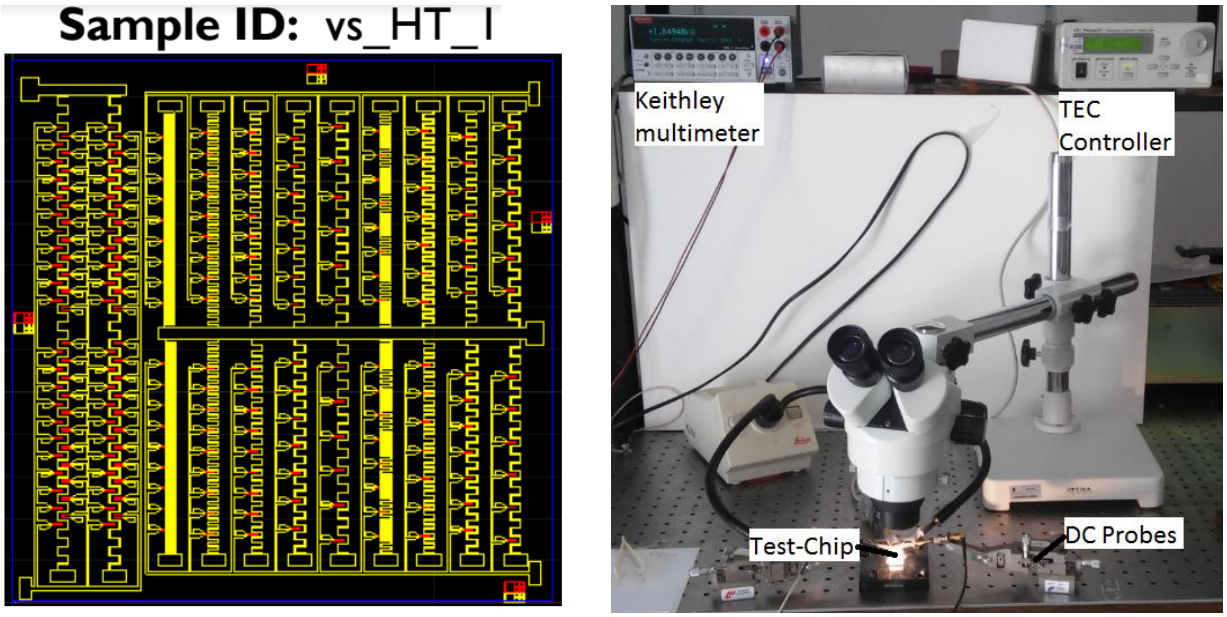

Figure 48- Ru sensors: Test-chip composed by Al heaters and Ru sensors manufactured at INESC-MN facilities [52] (left) and a photographic image of the testing setup (right).

The tests were performed in two samples of Ru sensors by varying the temperature, with temperature controller, from 15 °C to 65 °C in steps of 2 °C and measuring the Resistance as a function of temperature variation.

For each measured sample the temperature coefficient of electrical resistivity (TCR) [55] was calculated,

$$TCR = \left(\frac{dR}{dT}\right)/R_0 \tag{5.1}$$

where $\frac{dR}{dT}$ represents the derivative in T temperature and R_0 the room temperature resistance of the sensor.

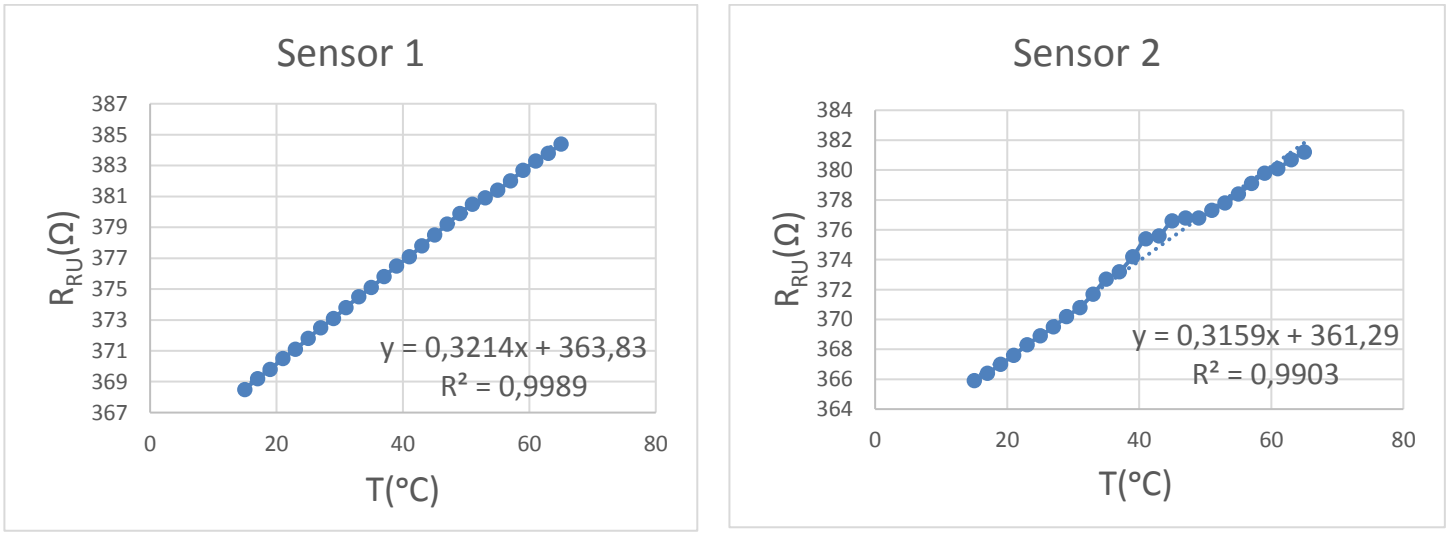

Figure 49 - Experimental resistance-to-temperature characteristic of two RU-sensors measured on test-chip.

By analyzing the graphs depicted in Figure 49, one can conclude that the results present a very good linearity, however both sensors present a low value of Resistance measured and an absolute sensitivity of 0.32 Ω/°C approximately which means that in this range of temperature the values of Resistance have increased only 16 Ω.

Based on Eq. (5.1), the TCR of each sample was calculated, and the values can be observed in Table 3.

	Ru-Sensor 1	Ru-Sensor 2
TCR (K^{-1})	0.864×10^{-3}	0.856×10^{-3}

Table 3 – Temperature coefficient of electrical resistivity calculated for both samples of RU-sensors.

These values of TCR are smaller than TCR for pure bulk RU, which is 4.2×10^{-3} K^{-1} [51], it means higher sensitivity to temperature variations.

5.2 Platinum and Titanium Temperature Sensors

This sub-chapter focuses on Platinum (Pt) and Titanium (Ti) based temperature sensors, which are thin film sensors composed by 250 Å thick Ti layer and a 1500 Å thick Pt layer deposited onto a 700 µm Si-substrate, a 3300 Å thick Alumina (Al_2O_3) layer for passivation and 500 Å thick Au for contact pads, see Figure 50, which are also fabricated using techniques adapted from integrated circuit manufacturing available at INESC-MN clean room facilities [52]. This type of thin film temperature sensor present application for wide temperature range, fabrication process controllability and low cost [55].

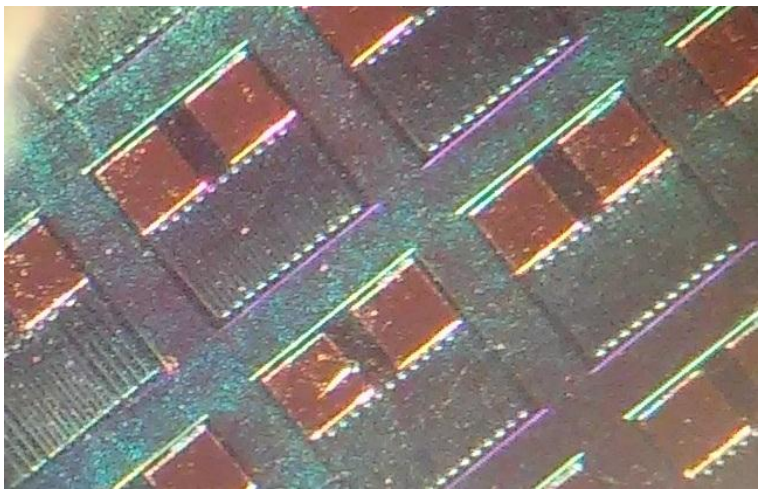

Figure 50 – Microscopic photograph of the Pt and Ti based temperature sensors.

5.2.1 PCB Design

In order to study the behavior of the sensors, it was needed a solution capable of offering better stability and reliability as at the same time facilitates the measurements and ensures better security for the chip. To fulfill these requirements a testing PCB was projected and designed using KICad EDA which is a free software that enables the design of schematics for electronic circuits and their conversion to PCB designs. The testing PCB is composed by twenty-eight pads and twenty eight ground-holes that match with the twenty-eight temperature sensors under testing. Figure 51 shows the 2D schematic design using KICad EDA.

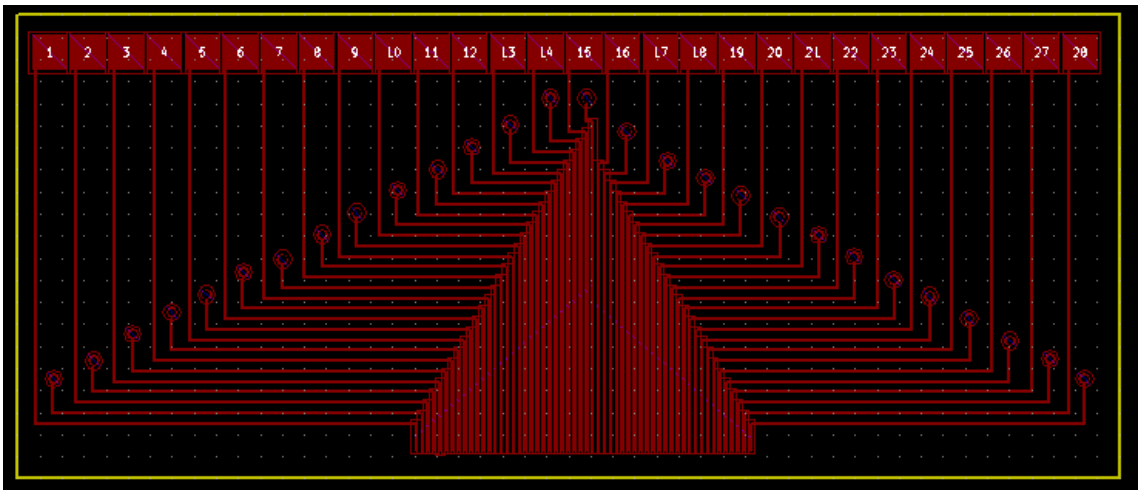

Figure 51 – Two dimensional PCB design using KICad.

It was then duplicated and attached onto a 65 mm x 60 mm aluminum plate, the chip with the sensors was then attached between the two PCB interfaces for contact wire-bonding as shown in figure 52.

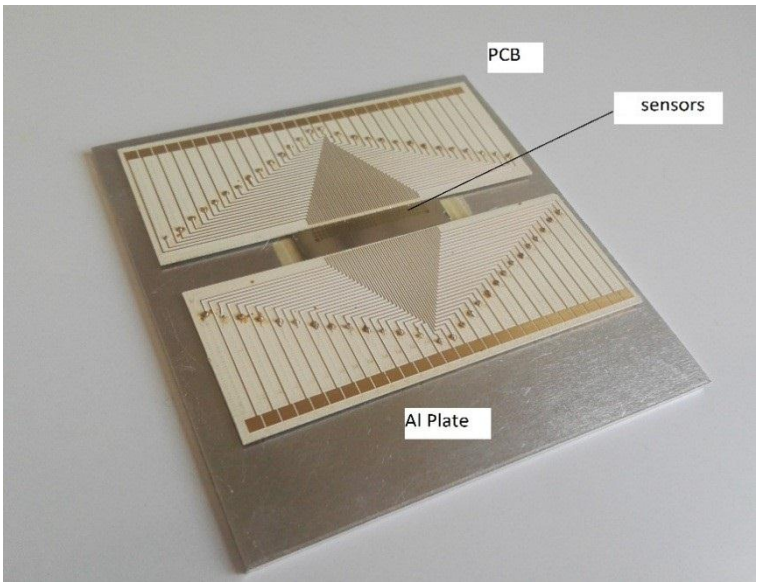

Figure 52 - Photographic image of Ru sensors test chip assembled onto the interface PCB.

5.2.2 Tests and Results

The chip under test consists of a thin Si-plate with the size of 5.6 mm x 19.5 mm which contains an array Pt and Ti based temperature sensors with the size of 500 µm x 500 µm with different characteristics, such as, length and the contact pads dimensions for bonding, which are described in table 4.

Sensor	Width (µm)	Length (µm)	Size (µm x µm)	Pad size (µm x µm)	Structure
TSCMW10L06090	10	6090	500 x 500	200 x 200	Round-corners
TSMW10L06090	10	6090	500 x 500	200 x 200	Square-corners
TSCMW10L07210	10	7210	500 x 500	200 x 200	Round-corners
TSMW10L07210	10	7210	500 x 500	200 x 200	Square-corners
TSCMW10L09190	10	9190	500 x 500	100 x 100	Round-corners
TSMW10L09190	10	9190	500 x 500	100 x 100	Square-corners
TSCMW10L11150	10	11150	500 x 500	100 x 100	Round-corners
TSMW10L11150	10	11150	500 x 500	100 x 100	Square-corners

Table 4 – Dimensions and structure of the Pt and Ti temperature sensors.

In order to measure the temperature dependency of resistance for Pt and Ti sensors, the setup described previously in Figure 48 (right) was used, however as the sensors have Au-based contact pads for wire-bonding, it was used the testing PCB depicted in Figure 52, instead of the DC-probes.

The tests were performed in one sample for each type of PT and Ti sensors by varying the temperature, with temperature controller, also from 15 ºC to 65 ºC in steps of 2 ºC and measuring the Resistance as a function of temperature variation.

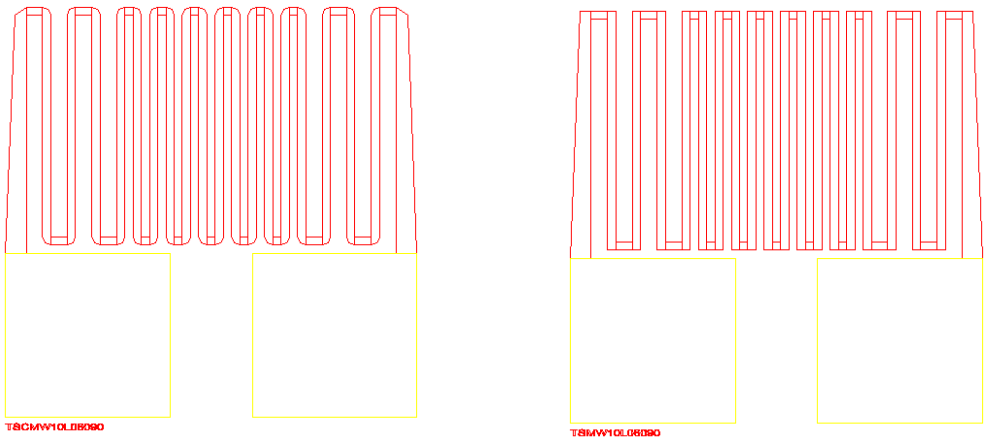

Figure 53 - Schematic of 10 x 6090 µm Ru-sensors: TSCMW10L06090 with round corners (left) and TSMW10L06090 with square corners (right).

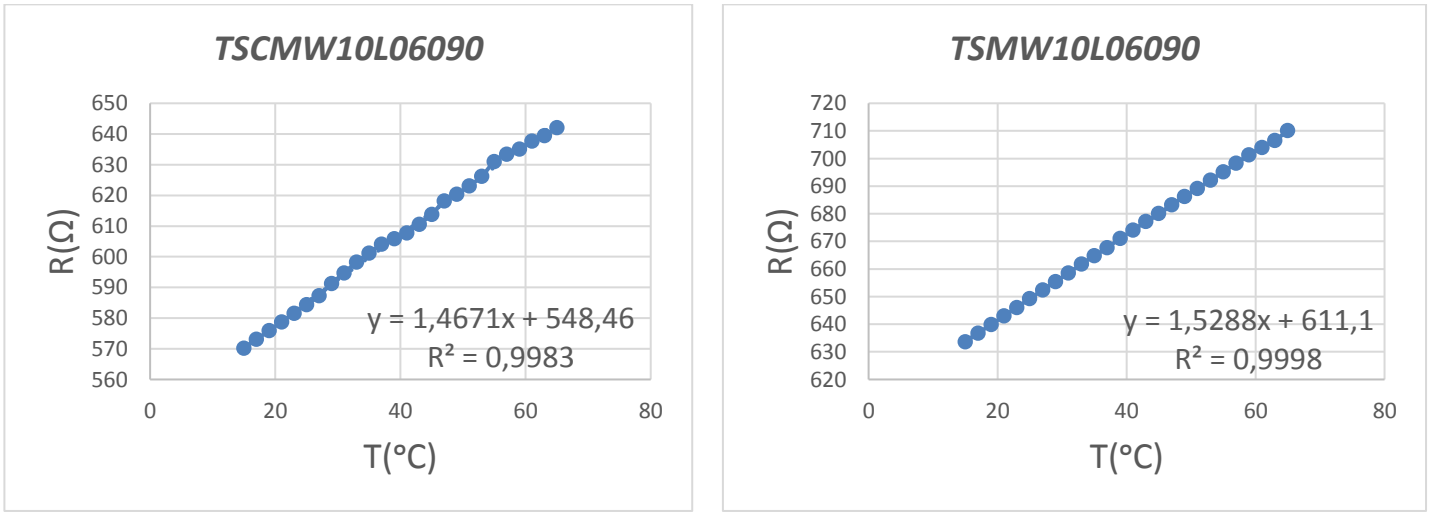

Figure 54 - Experimental resistance-to-temperature characteristic of TSCMW10L06090 (left) and TSMW10L06090 (right).

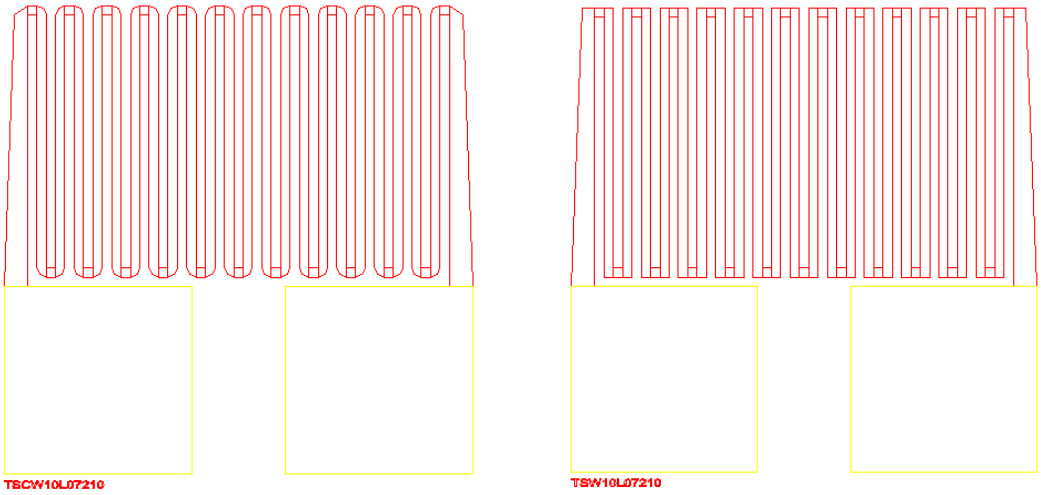

Figure 55 - Schematic of 10 x 7210 µm Ru-sensors: TSCMW10L07210 with round corners (left) and TSMW10L07210 with square corners (right).

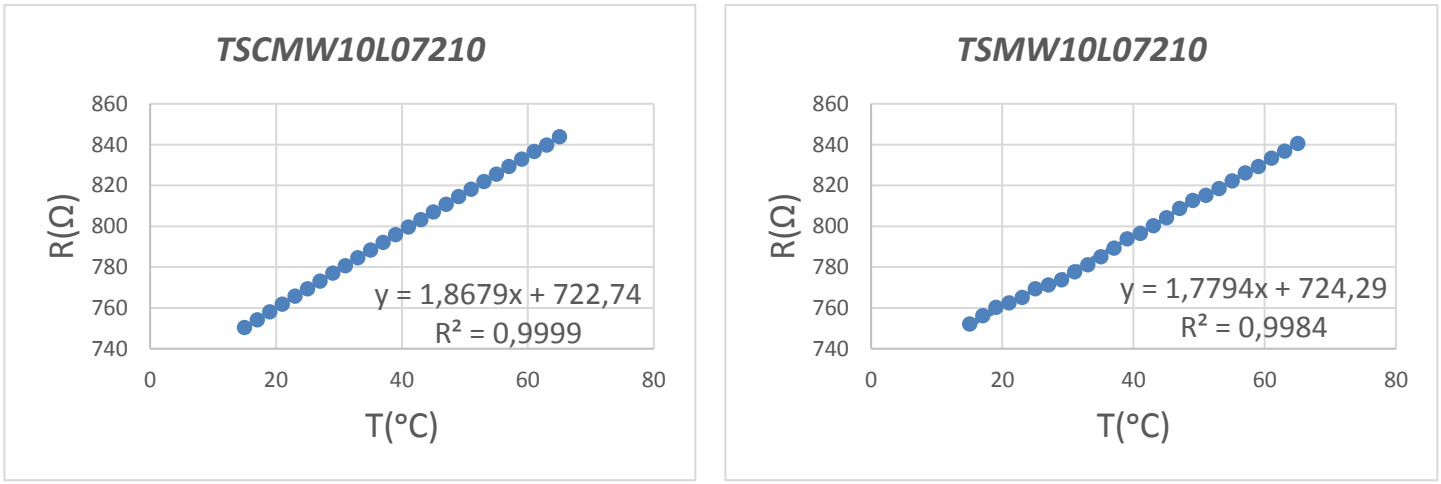

Figure 56 - Experimental resistance-to-temperature characteristic of TSCMW10L07210 (left) and TSMW10L07210 (right).

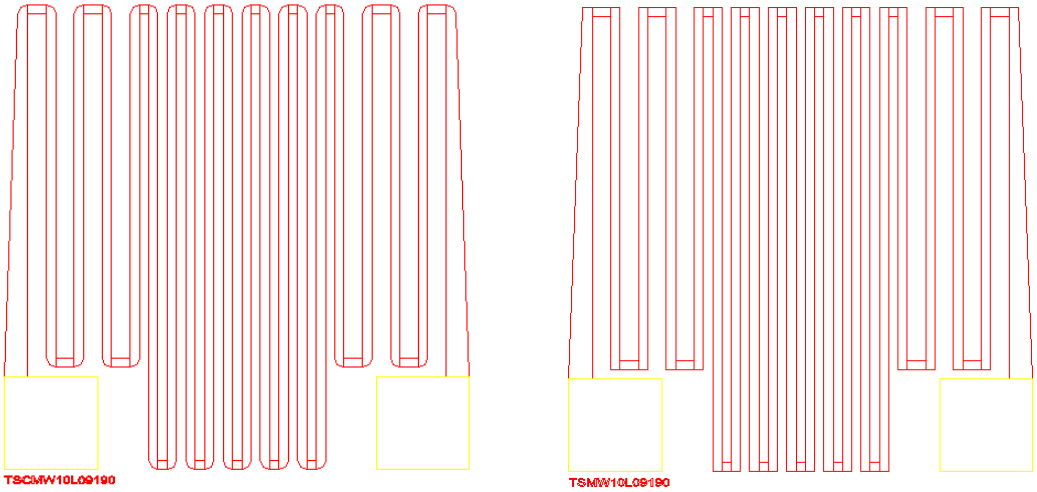

Figure 57 - Schematic of 10 x 9190 µm Ru-sensors: TSCMW10L09190 with round corners (left) and TSMW10L09190 with square corners (right).

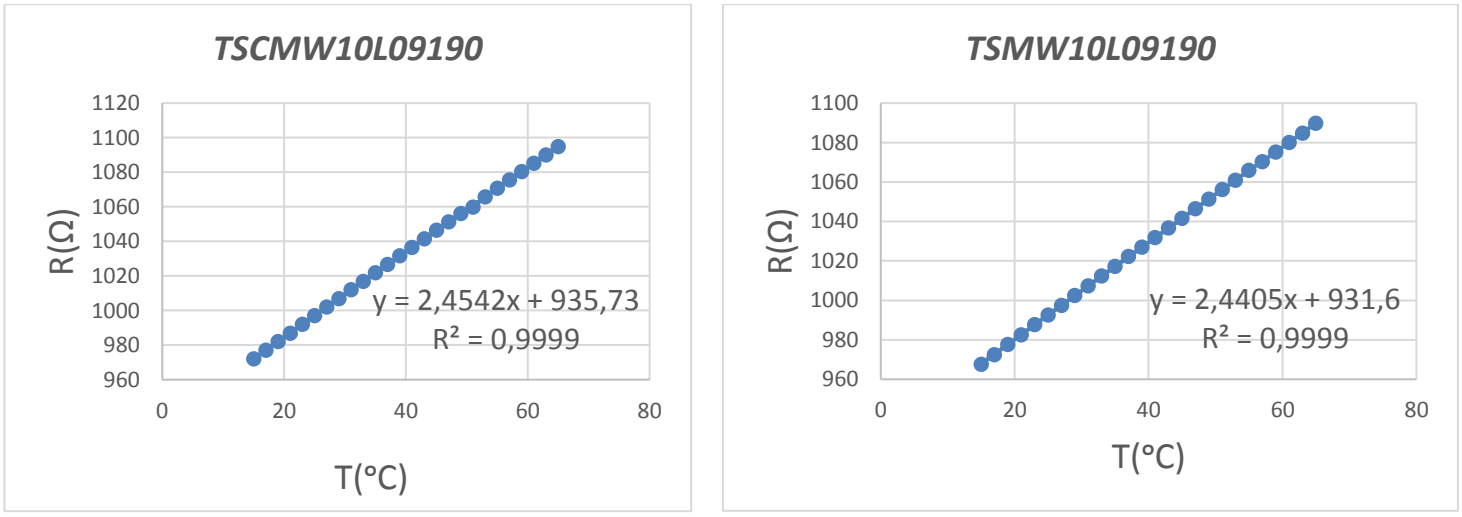

Figure 58 - Experimental resistance-to-temperature characteristic of TSCMW10L09190 (left) and TSMW10L09190 (right).

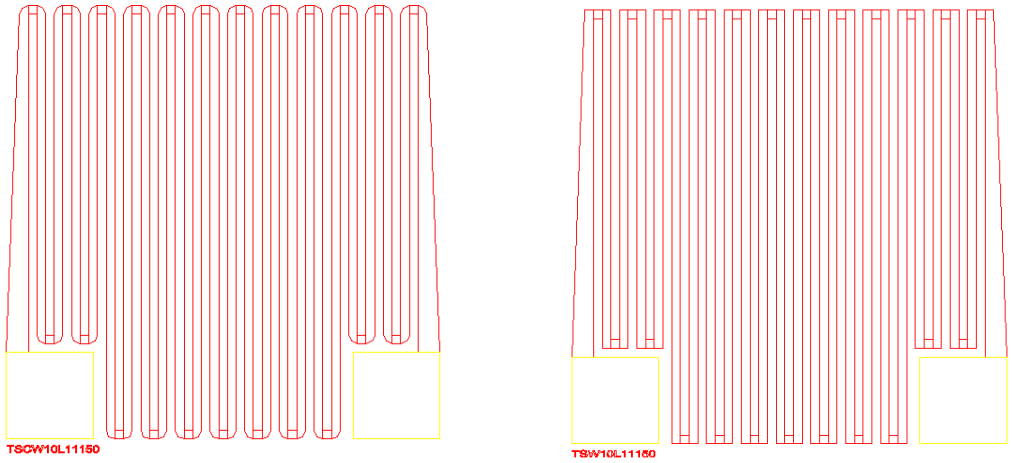

Figure 59 - Schematic of 10 x 9190 µm Ru-sensors: TSCMW10L11150 with round corners (left) and TSMW10L11150 with square corners (right).

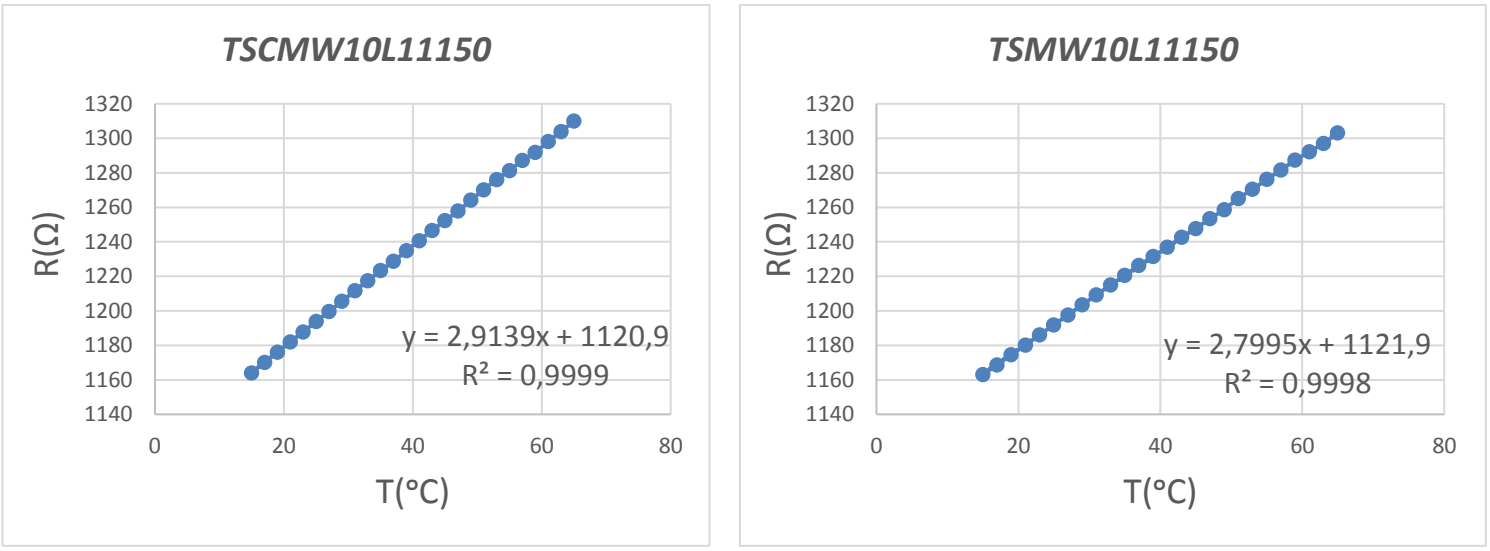

Figure 60 - Experimental resistance-to-temperature characteristic of TSCMW10L11150 (left) and TSMW10L11150 (right).

By the analysis of the previous graphs depicted in Figures 54-60, one can observe that the results present good linearity. By comparison with Ru-sensors approached previously, one can conclude that Pt and Ti sensors can achieve higher values of Resistance at the same range of temperature, the sensitivity is also higher which means a larger increase of the resistance values. In terms of structure there is no significant differences between the results of the samples with round- and square-corners, which means that the structure does not have a significant impact on the sensitivity to temperature.

One can also observe that the larger the sensor length, the greater the measured resistance and sensitivity presenting a linear evolution, see Figure 61.

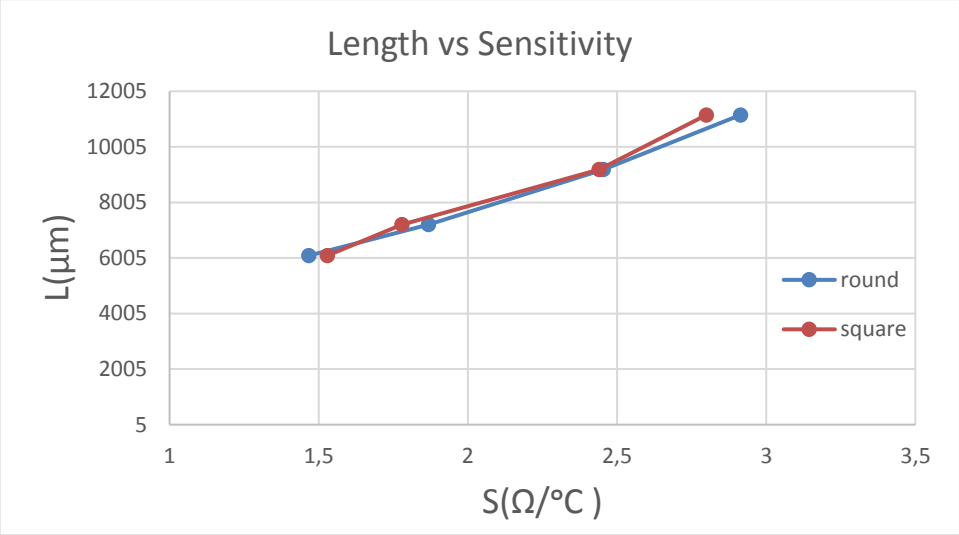

Figure 61 - Evolution of the sensitivity as a function of the length of the sensors.

Based on Eq. (5.1), the TCR of each sample was calculated, and the values can be observed in Table 5.

Sensor	TCR (K^{-1})
TSCMW10L06090	2.51×10^{-3}
TSMW10L06090	2.35×10^{-3}
TSCMW10L07210	2.46×10^{-3}
TSMW10L07210	2.38×10^{-3}
TSCMW10L09190	2.46×10^{-3}
TSMW10L09190	2.44×10^{-3}
TSCMW10L11150	2.44×10^{-3}
TSMW10L11150	2.30×10^{-3}

Table 5 - Temperature coefficient of electrical resistivity calculated for all samples of Pt and Ti sensors.

These TCR values are smaller than the standard TCR for pure bulk Pt which is $3.9 \times 10^{-3}\ K^{-1}$, meaning higher sensitivity to temperature variations. One can also conclude, by analyzing table 5, that the sensors with square-corner structure present smaller values of TCR, although there is no significant difference, it can be said that in this case the sensors with square-corners have more sensitivity to temperature variations than those with round-corners.

The sensors with higher length, *TSCMW10L11150* and *TSMW10L11150*, with round- and square-corners respectively, present the lower value of TCR as well as the higher resistance.

6 Conclusions and Future Work

6.1 Conclusions

The Photonic Packaging technology has been increased for the past years in order to address the low cost and better performance requirements. The main objective of this work was to present an overview on the evolution of photonic packaging rules and techniques during the years, proposing at the same time from a practical point of view, some alternatives in order to address the packaging improvement needs for the next-generation PIC's.

The Photonic Packaging process is divided by three main different areas the optical, electrical and thermal management and initially in this document a theoretical overview was given for each of them.

For the optical packaging a fiber-to-chip coupling implementation based in manufactured ball-lensed fibers was tested using a test-chip and manufactured holder with a DFB laser. By using ball-lensed fibers instead of a non-lensed fiber one can achieve MOP improvement of approximately 2 dB, it also allows for a less time consuming and efficient fiber-to-chip active alignment, it also offers a lower optical power variation in response to a slight lateral and vertical misalignment, which proves to be a major improvement for optical packaging. One can also affirm that small ball-lensed diameters offer better MOP, however they have more stringent adjusting tolerances. For fiber-to-chip alignment the Si-holders with V-grooves fabrication was performed using techniques adapted from integrated circuit manufacturing at INESC-MN clean room facilities, two sets of Si-holders were manufactured in two Si-wafers, one with a 90º dicing and the other one with a 21º dicing and the final results show that the one with the 90º dicing has some structural deformations in the v-grooves which means that the fabrication process for this one must be repeated further.

For the electrical packaging two bonding techniques were studied and discussed for electronic connections between the EIC and the PIC and between the PIC and a PCB substrate, which are Wire-bonding and Flip-Chip. A characterization of the s-parameters of a testing PIC with wire-bonding was performed and the

results show the total reflection as predictable, however have some peaks which can be explained by the different width of the RF-lines between the RF-connectors and the chip along their length which cause more losses meaning that these RF-lines are not completely adapted.

The last chapter in this document focuses on thermal management which explores the study of two different types of temperature sensors, one is ruthenium-based and the other is platinum- and titanium-based sensors. A testing-PCB was designed in order to measure the temperature dependency of resistance for Pt and Ti sensors. The same measurements were performed for Ru-based sensors but with DC-probes instead of a PCB. The results present good linearity as expected. By comparison with Ru-sensors, one can conclude that Pt and Ti sensors can achieve higher values of Resistance at the same range of temperature, the sensitivity is also higher which means a larger increase of the resistance values.

The TCR calculated values for both types of sensors are smaller than the standard TCR for pure bulk Pt and for pure bulk Ru which means higher sensitivity to temperature variations.

6.2 Future work

As future work, for optical packaging a study based on different lensed-fiber tips should be made and tested.

For electrical packaging the Flip-Chip bonding technique should be implemented and tested, the s-parameter characterization should also be made and compared with the results achieved with wire-bonding technique.

A prototype package follow the standard “butterfly package” according with the characteristics and specifications of the developed PIC’s should be manufactured.

References

[1]. Fischer-Hirchert, Ulrich HP. "Introduction into Photonic Packaging." Photonic Packaging Sourcebook. Springer Berlin Heidelberg, 2015. 1-21.

[2]. Mason, Analysys. "Fibre capacity limitations in access networks." Report for OFCOM (2010).

[3]. Lee, Jun Su, et al. "Meeting the electrical, optical, and thermal design challenges of photonic-packaging." IEEE Journal of Selected Topics in Quantum Electronics 22.6 (2016): 409-417.

[4]. Nicola Pavarelli, Peter A. O'Brien and Jun Su Lee. "Packaging Challenges for Integrated Silicon Photonics Circuits", Tyndall National Institute, Cork, Ireland, March-2016.

[5]. Carroll, Lee, et al. "Photonic Packaging: Transforming Silicon Photonic Integrated Circuits into Photonic Devices." Applied Sciences 6.12 (2016): 426.

[6]. Azadeh, M. (2009). "Fiber optics engineering" (p. 179-180). Springer.

[7]. Karioja, Pentti, et al. "Comparison of active and passive fiber alignment techniques for multimode laser pigtailing." Electronic Components & Technology Conference, 2000. 2000 Proceedings. 50th. IEEE, 2000.

[8]. Fischer, Ulrich HP. "Opto-Electronic Packaging". INTECH Open Access Publisher, 2013.

[9]. Rogner, A., et al. "LIGA-based flexible microstructures for fiber-chip coupling." Journal of Micromechanics and Microengineering 1.3 (1991): 167.

[10]. Cohen, Mitchell S., et al. "Packaging of high density fiber/laser modules using passive alignment techniques." IEEE transactions on components, Hybrids, and Manufacturing Technology 15.6 (1992): 944-955.

[11]. Hashimoto, Toshikazu, et al. "Hybrid integration of spot-size converted laser diode on planar lightwave circuit platform by passive alignment technique." IEEE Photonics Technology Letters 8.11 (1996): 1504-1506.

[12]. Lee, Sang-Hwan, et al. "Optical device module packages for subscriber incorporating passive alignment techniques." Electronic Components and Technology Conference, 1995. Proceedings, 45th. IEEE, 1995.

[13]. Roelkens, Günther, et al. "Grating-based optical fiber interfaces for silicon-on-insulator photonic integrated circuits." IEEE Journal of Selected topics in quantum Electronics 17.3 (2011): 571-580.

[14]. EPIC, “Packaging Design Rules for Si- & InP-Photonics”, DRAFT 1.0, March 2015

[15]. LINKRA, “Design Rules For Photonic Packaging”, 2016

[16]. TYNDALL, “Design Rules for Silicon Photonic Packaging at Tyndall Institute”, January 2015

[17]. Taillaert, Dirk, et al. "Grating couplers for coupling between optical fibers and nanophotonic waveguides." Japanese Journal of Applied Physics 45.8R (2006): 6071.

[18]. McNab, Sharee J., Nikolaj Moll, and Yurii A. Vlasov. "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides." Optics express 11.22 (2003): 2927-2939.

[19]. Romero-Garcia, Sebastian, et al. "Edge couplers with relaxed alignment tolerance for pick-and-place hybrid integration of III–V lasers with SOI waveguides." IEEE Journal of Selected Topics in Quantum Electronics 20.4 (2014): 369-379.

[20]. University of Twente, “Photonic packaging and integration technologies I”, Winter College on Optics: Fundamentals of Photonics - Theory, Devices and Applications, February 2014.

[21]. Worhoff, Kerstin, et al. "Flip-chip assembly for photonic circuits." Photonics Europe. International Society for Optics and Photonics, 2004.

[22]. Zhang, X. R., et al. "Copper pillar bump structure optimization for flip chip packaging with Cu/Low-K stack." Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE), 2010 11th International Conference on. IEEE, 2010.

[23]. T. Baehr-Jones et al., “Myths and rumours of silicon photonics,” Nature Photon., vol. 6, pp. 206–208, 2012.

[24]. Sharma, Sudhanshu, V. K. Dwivedi, and S. N. Pandit. "A review of thermoelectric devices for cooling applications." International Journal of Green Energy 11.9 (2014): 899-909.

[25]. Edwards, Christopher A., Herman M. Presby, and Corrado Dragone. "Ideal microlenses for laser to fiber coupling." Journal of Lightwave Technology 11.2 (1993): 252-257.

[26]. Van Zantvoort, Johan HC, et al. "Lensed fiber-array assembly with individual fiber fine positioning in the submicrometer range." IEEE Journal of selected topics in quantum electronics 12.5 (2006): 931-939.

[27]. Zheng, Wenxin. "Optic lenses manufactured on fiber ends." Optoelectronics Global Conference (OGC), 2015. IEEE, 2015.

[28]. Pinho, Cátia, et al. "Characterization of an InP Asymmetric Coupler". Paper submitted to ECOC 2017 Conference, 2017.

[29]. Ghafouri-Shiraz, H. "Distributed feedback laser diodes and optical tunable filters". John Wiley & Sons, 2004.

[30]. G. P. Agrawal, "Fiber-optic communication systems", 3rd Ed.. John Wiley & Sons, 2002.

[31]. Carroll, John E., James Whiteaway, and Dick Plumb. "Distributed feedback semiconductor lasers". Vol. 10. IET, 1998.

[32]. Mailly, Dominique, and Christophe Vieu. "Lithography and etching processes." Nanoscience. Springer Berlin Heidelberg, 2007. 3-40.

[33]. C. A. Mack. "Field Guide to Optical Lithography". SPIE Press, Bellingham, WA (2006).

[34]. Fischer-Hirchert, Ulrich HP. "Passive Adjustment Techniques." Photonic Packaging Sourcebook. Springer Berlin Heidelberg, 2015. 206-216.

[35]. Chen, Yang-Yuan, et al. "Fabrication, characterization and thermal properties of nanowires". INTECH Open Access Publisher, 2011.

[36]. Mozooni, Babak. (June 2015). Optical Lithography. TECHOMAT. Retrieved from https://techomat.com.

[37]. Li, Nianzhen, Anna Tourovskaia, and Albert Folch. "Biology on a chip: microfabrication for studying the behavior of cultured cells." Critical Reviews™ in Biomedical Engineering 31.5&6 (2003).

[38]. Betancourt, Tania, and Lisa Brannon-Peppas. "Micro-and nanofabrication methods in nanotechnological medical and pharmaceutical devices." International journal of nanomedicine 1.4 (2006): 483.

[39]. Franssila, Sami. "Introduction to microfabrication". John Wiley & Sons, 2010.

[40]. Chen, Kuo-Shen, et al. "Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)." Journal of Microelectromechanical Systems 11.3 (2002): 264-275.

[41]. Harman, George G. “Wire bonding in microelectronics”. McGraw-Hill, 2010.

[42]. Fischer-Hirchert, Ulrich HP. "Soldering, Adhesive Bonding, and Bonding." Photonic Packaging Sourcebook. Springer Berlin Heidelberg, 2015. 133-147.

[43]. Lau, John H. "Cost analysis: solder bumped flip chip versus wire bonding." IEEE Transactions on Electronics Packaging Manufacturing 23.1 (2000): 4-11.

[44]. Valenta, Václav, et al. "Design and experimental evaluation of compensated bondwire interconnects above 100 GHz." International Journal of Microwave and Wireless Technologies 7.3-4 (2015): 261-270.

[45]. Spaan, E., et al. "Wire bonding the future: a combined experimental and numerical approach to improve the Cu-wire bonding quality." Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE), 2010 11th International Conference on. IEEE, 2010.

[46]. Gehman, Bruce. "Bonding wire microelectronic interconnections." IEEE Transactions on Components, Hybrids, and Manufacturing Technology 3.3 (1980): 375-383.

[47]. Zhang, Zhuqing, Pengli Zhu, and C. P. Wong. "Flip-Chip Underfill: Materials, Process, and Reliability." Materials for Advanced Packaging. Springer International Publishing, 2017. 331-371.

[48]. Elenius, Peter, and Lee Levine. "Comparing flip-chip and wire-bond interconnection technologies." Chip Scale Review 4.6 (2000).

[49]. Chen, Shoulung, et al. "Mechanical behavior of flip chip packages under thermal loading." Electronic Components and Technology Conference, 2005. Proceedings. 55th. IEEE, 2005.

[50]. National Center for Biotechnology Information. PubChem Compound Database; CID=23950, https://pubchem.ncbi.nlm.nih.gov/compound/23950 (accessed May. 31, 2017).

[51]. The PGM. Database, http://www.pgmdatabase.com.

[52]. Silvério, V., et al. "Design, fabrication and test of an integrated multi-microchannel heat sink for electronics cooling." Sensors and Actuators A: Physical 235 (2015): 14-27.

[53]. Lopes, António, et al. "MgO magnetic tunnel junction electrical current sensor with integrated Ru thermal sensor." IEEE Transactions on Magnetics 49.7 (2013): 3866-3869.

[54]. Ravelo Arias, S. I., et al. "Ru-based thin film temperature sensor for space environments: microfabrication and characterization under total ionizing dose." Journal of Sensors 2016 (2016).

[55]. Jiang, Shui-Dong, et al. "Microfabrication of thin film temperature sensor for cryogenic measurement." Microsystem technologies 20.3 (2014): 451-456.